
xTCA for Physics Standards Progress & Applications Summary for Project X Collaboration September 11-12, 2009

Ray Larsen
SLAC National Accelerator Laboratory
ARD-LC Department

Outline

I. PICMG xTCA for Physics Standards Committee Roadmaps

- Hardware & Software WG's
- http://www.picmg.org/pdf/PICMG_Physics_Public_Web_Update_061209_R5-3.pdf

II. Accelerator Applications

- DESY XFEL, SLAC Controls Upgrade

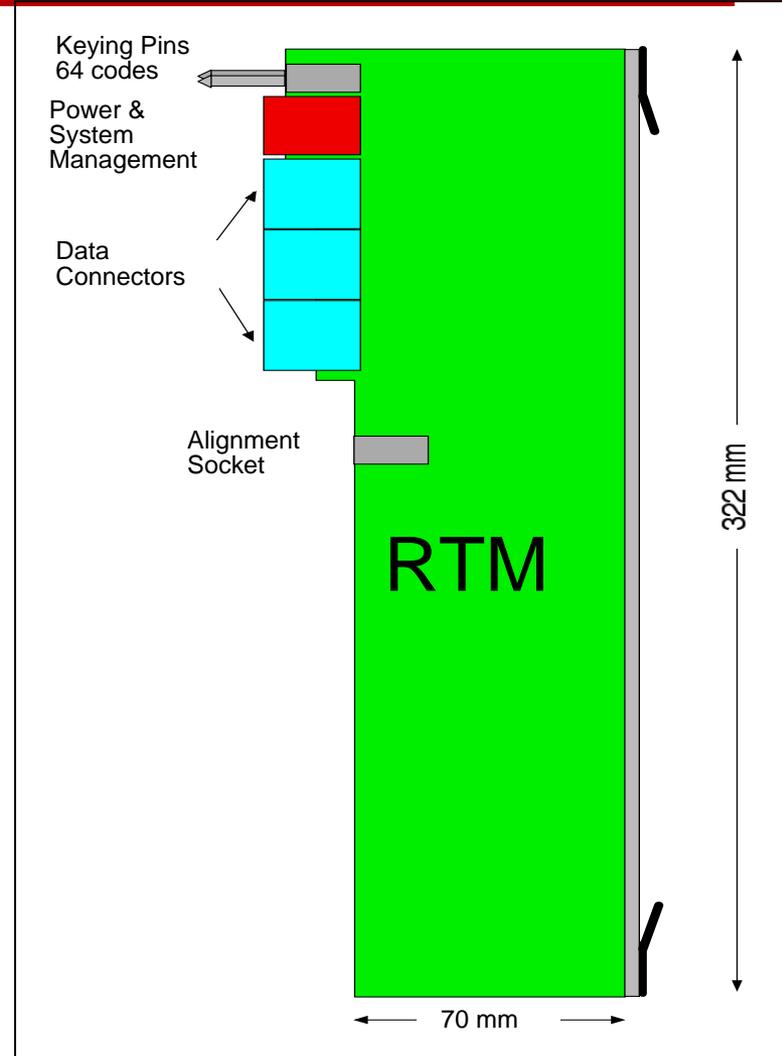
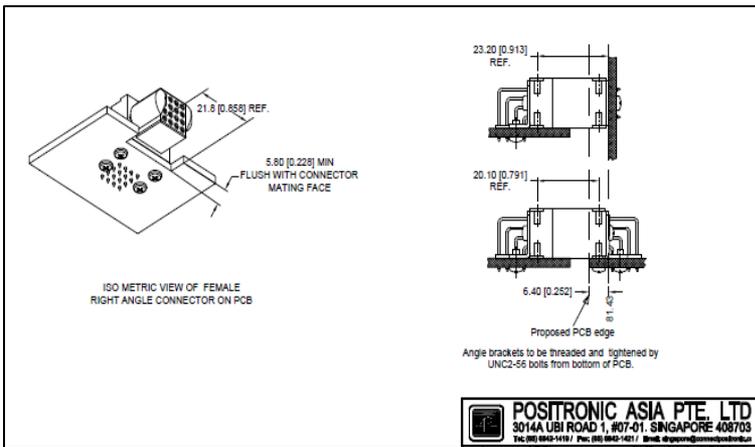
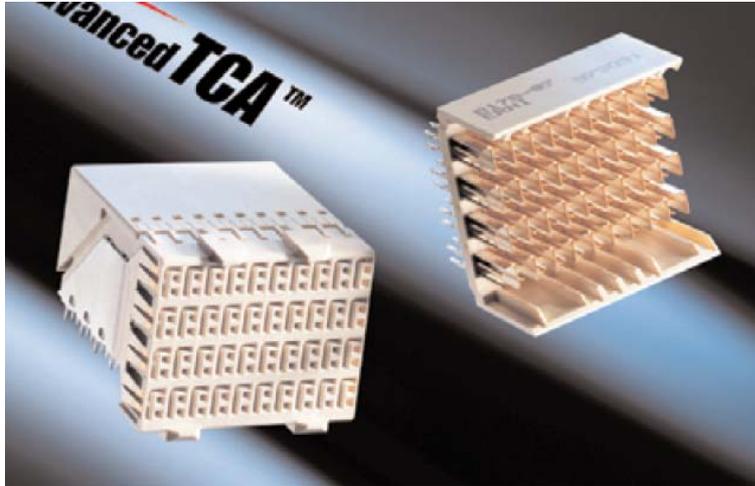
I. Committee Roadmaps

- Adapt xTCA for physics use
 - Extensions to specifications
 - Guidelines
 - Open source solutions
 - Build on existing xTCA base under PICMG rules
 - Approval by PICMG membership vote
 - Collaborate with industry for vendor support

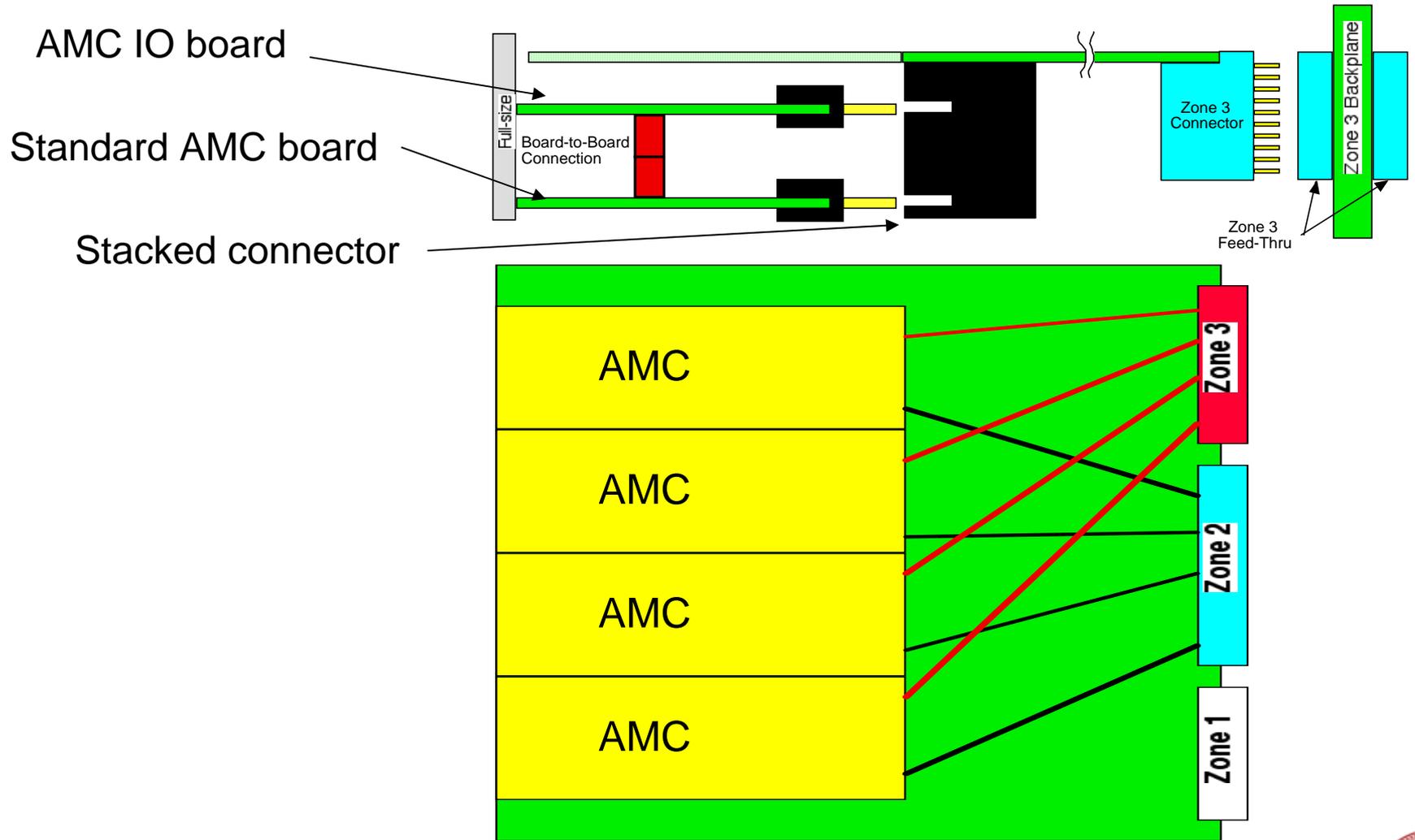
Hardware WG1 Roadmap

- Sub-Projects Approved for Roadmap
 1. ATCA Rear Transition Module Interface for IO
 2. ATCA Carrier Boards for AMC's w/ Rear IO (2)
 3. AMC (Advanced Mezzanine Cards) w/Rear IO (2)
 4. MTCA (MicroTCA) Chassis w/ Rear IO (2)
 5. ATCA/MTCA Clock & Trigger Distribution

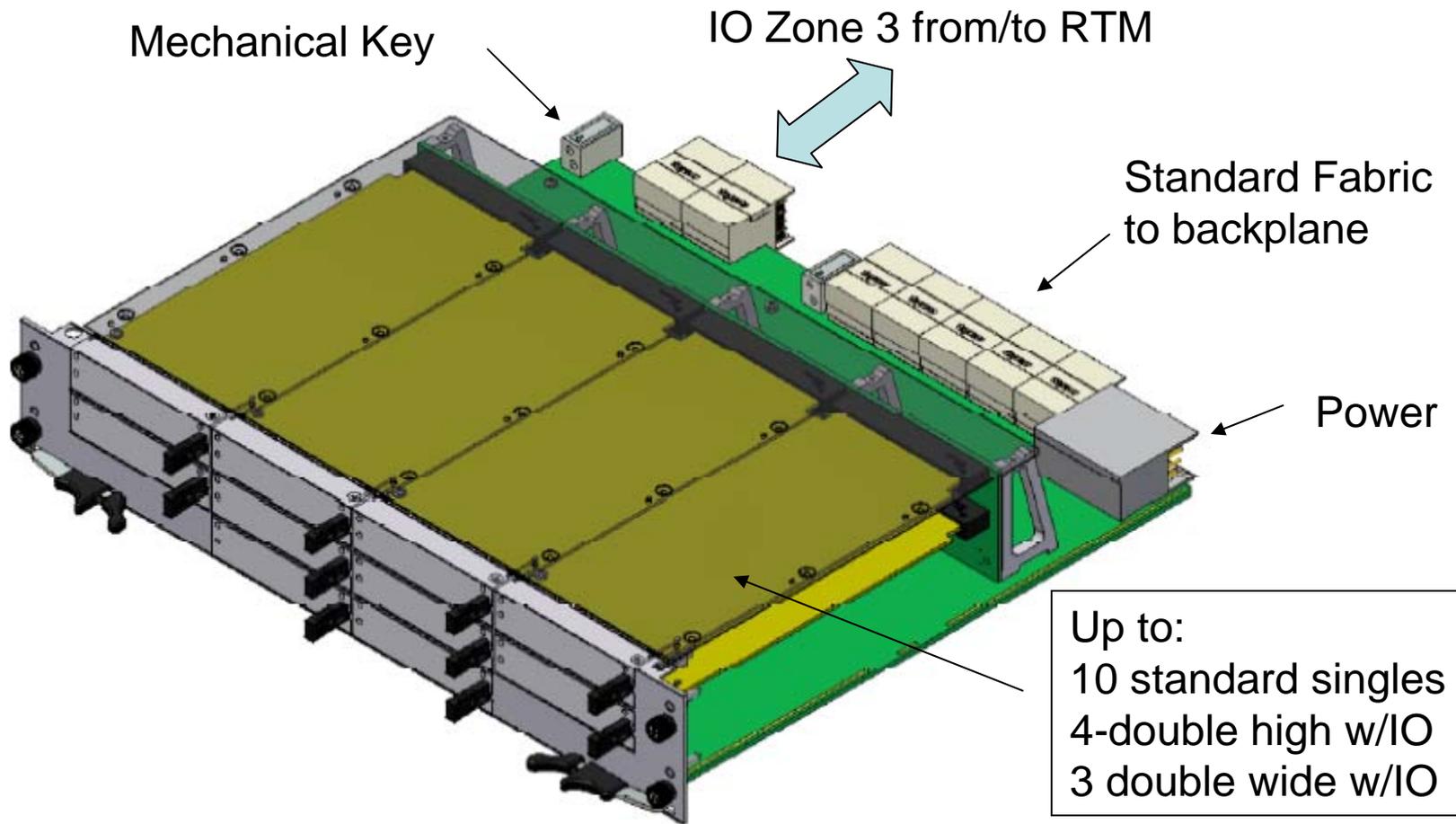
1. ATCA RTM Zone 3 Concept



2a. Carrier w/ Stacked AMC's IO (DESY)



2b. Carrier Concept for 1 or 2- Wide AMC

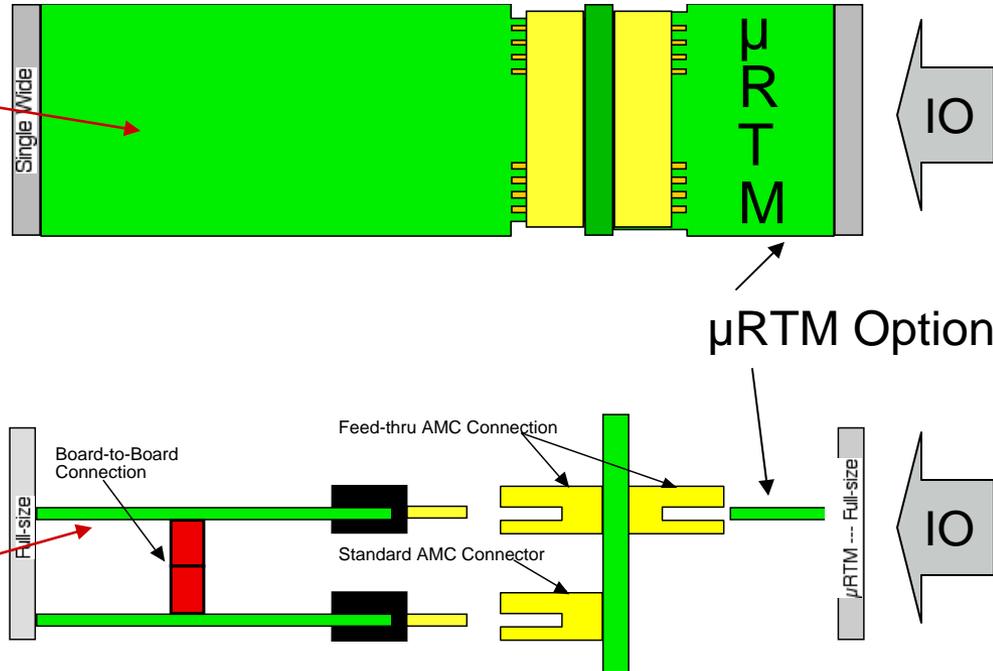


3a. Stacked 1-wide AMC w/ IO

(From DESY LLRF Design)

- Stacked AMC Board(s)

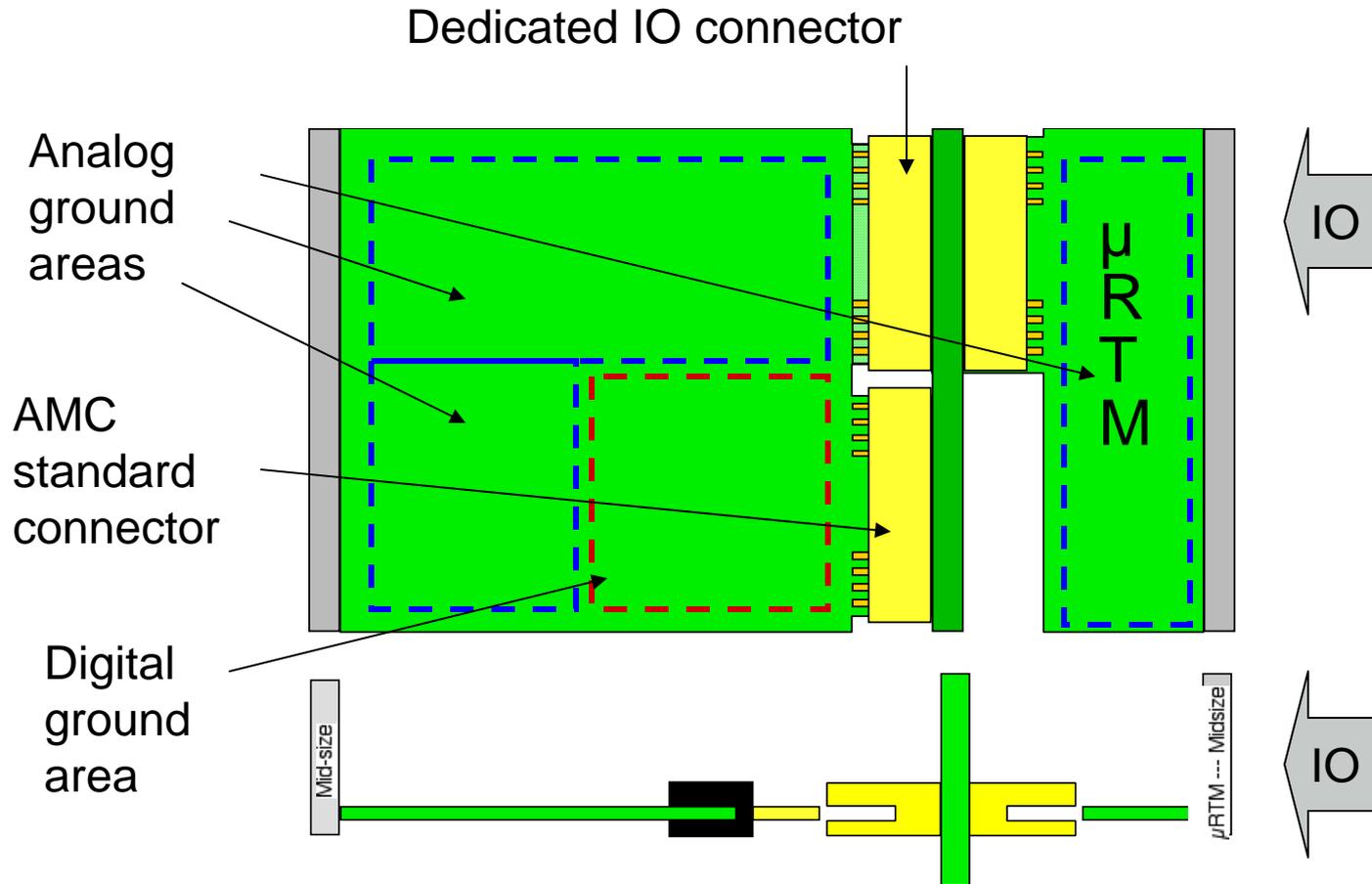
- Stacked boards and connector
- IO confined to second board
- Superior analog grounding, shielding, crosstalk isolation



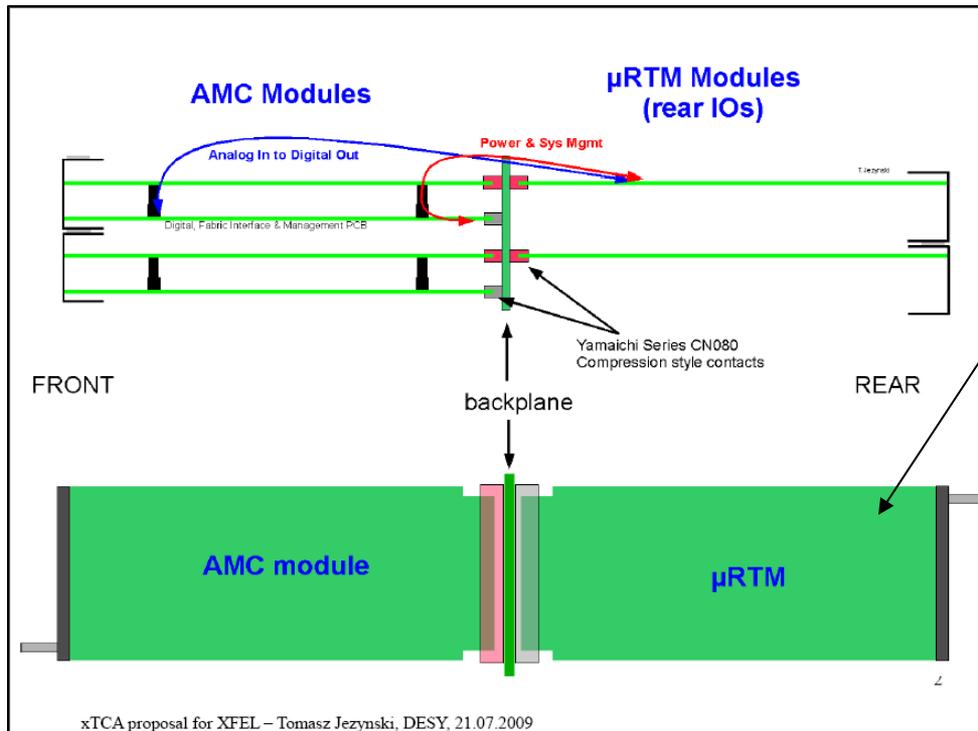
Dwg. Courtesy R. Downing, SLAC

3b. 2-Wide AMC w/IO

(Design for Carrier or MTCA w/ Rear IO)

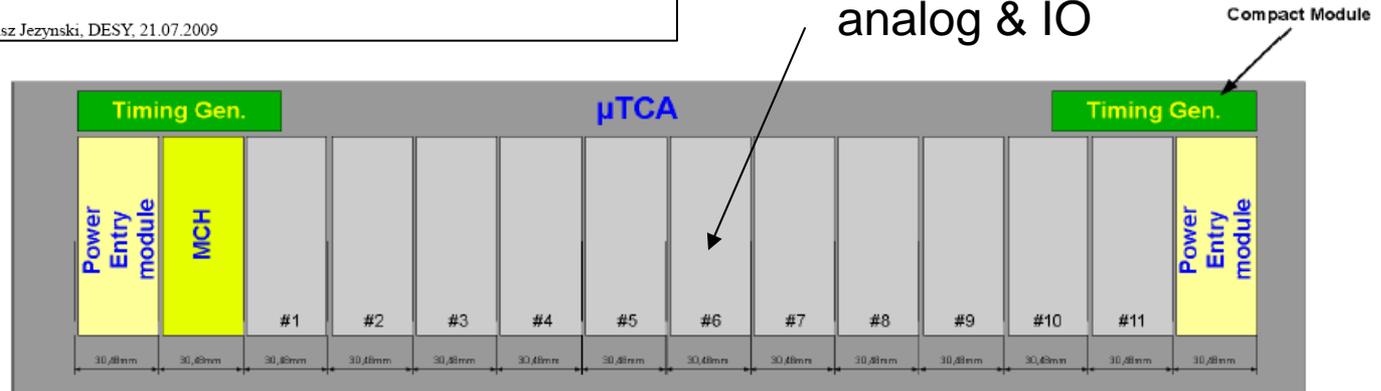


4a. 1-Wide Stacked AMC in MTCA

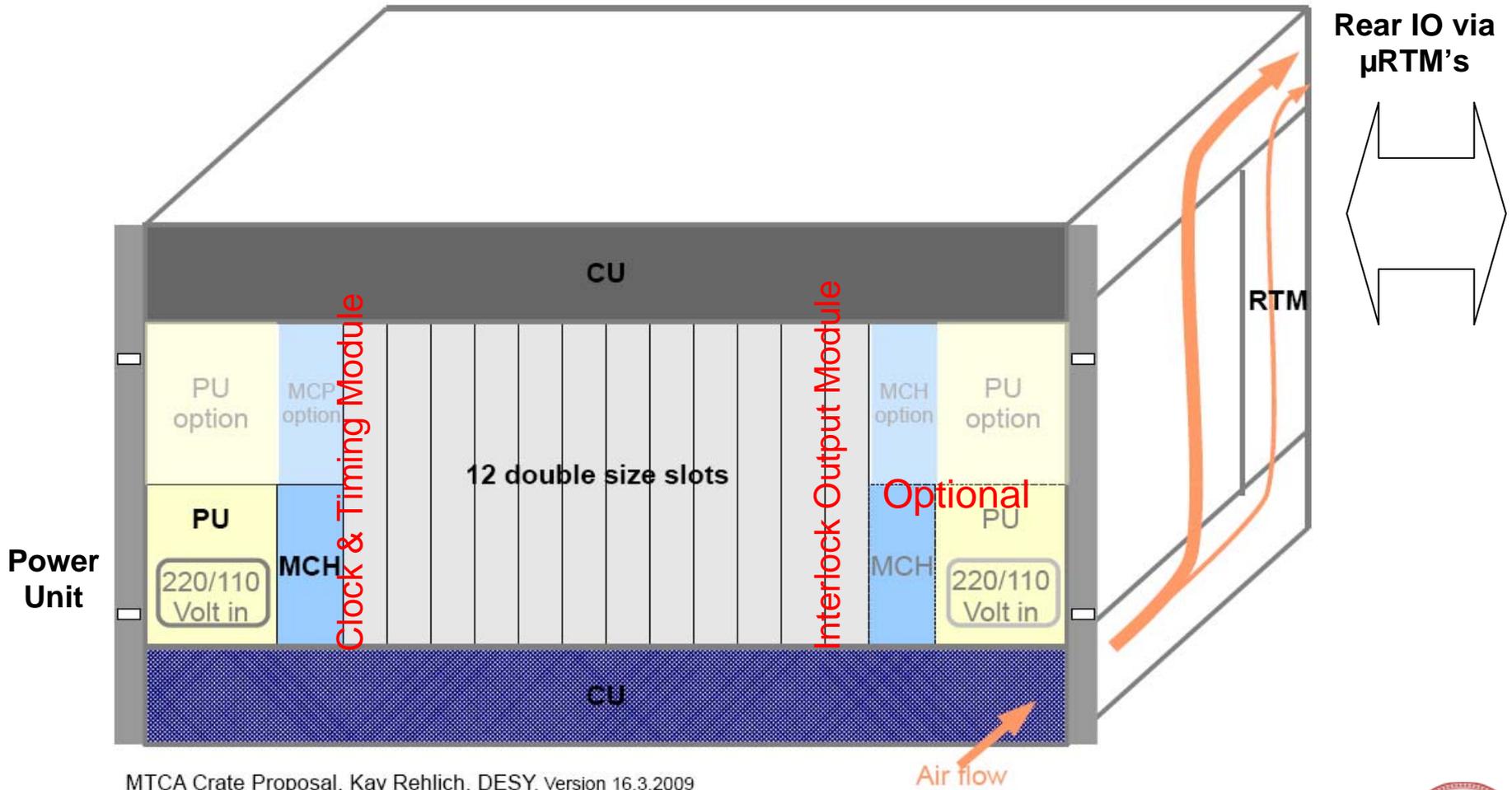


Full size RTM option

AMC Panels 2-high (vs. 1.5) w/ alternate slots dedicated to analog & IO



4b. 2-Wide 12 Payload AMC MTCA



MTCA Crate Proposal, Kay Rehlich, DESY, Version 16.3.2009

5a. Clocks & Triggers in ATCA

- Backplane clock & trigger dist'n needed for ease in hot swap
- Star buffered fanout needed to avoid timing disruption to neighbor modules on hot-swap
- Extended options region dual star lines in std backplane available
- Use lines for slots 15-16 (not needed for standard 14-slot crate)
- Incorporate timing buffers in separate module or switch modules for redundant system

Software WG2 Roadmap

- Major Software WG2 goals
 - Explore software systems for physics for *high interoperability, availability* and *performance* solutions across laboratories
 - Explore existing ATCA open-source software developments for potential use in high availability physics systems
 - Develop common guidelines for real time low latency protocols for fast synchronized systems (e.g. intra-pulse RF feedback control)
 - Develop generic API's for analog-digital applications to reduce development time, enhance interoperability

Software WG2 Road Map 2

- Interoperability
 - Develop Generic API's and Protocols for:
 - Management of real-time DAQ & machine control components
 - High rate & low latency transactions
 - Management of resources within xTCA network
- Availability
 - Define mechanisms for management of redundancy, hot swap and auto-failover
 - Develop IPMI architecture to include LAN access for managing distributed FPGA controls environment
- Performance
 - Standardize environment, use available standards to save development time
 - Efficient communications from high speed point-to-point to full network levels

Software WG2 Progress

- Tutorials
 - Series of tutorials from industry and lab experts ongoing
 - IPMI, HPM1.1, LAN-based IPMI, SRIO & PCIe vs. GbE protocols, OpenSAF etc.
- Generic API's for physics
 - Framework proposed for Embedded Machine Control Protocol for physics
 - Includes integration of features found in various standards optimized for physics (e.g. VXI, SCPI, IVI...)
 - Includes virtual ADC example of hardware independent specification
- Prototyping Experience
 - Study of ongoing systems initiatives at DESY, SLAC, IPFN (JET & ITER) to help frame requirements, provide test beds

Standards Summary Status

- All above projects being worked at concept level.
- Priorities
 1. ATCA RTM – Draft spec underway
 2. AMC Single wide 2-stack AMC's – Prototype working (DESY)
 3. AMC Double wide w/ μ RTM – Detailed design near cmplt. (DESY)
 4. ATCA 2-stack Carrier – Prototype working (DESY)
 5. MTCA 2-wide chassis w/ μ RTM – Design near complete (Schroff)
 6. MTCA 1-wide stacked AMC w/ μ RTM – Concept stage
- Goal: Specs, prototypes Q4 2009-Q2 2010
- Spec approvals: Q2-Q3 2010

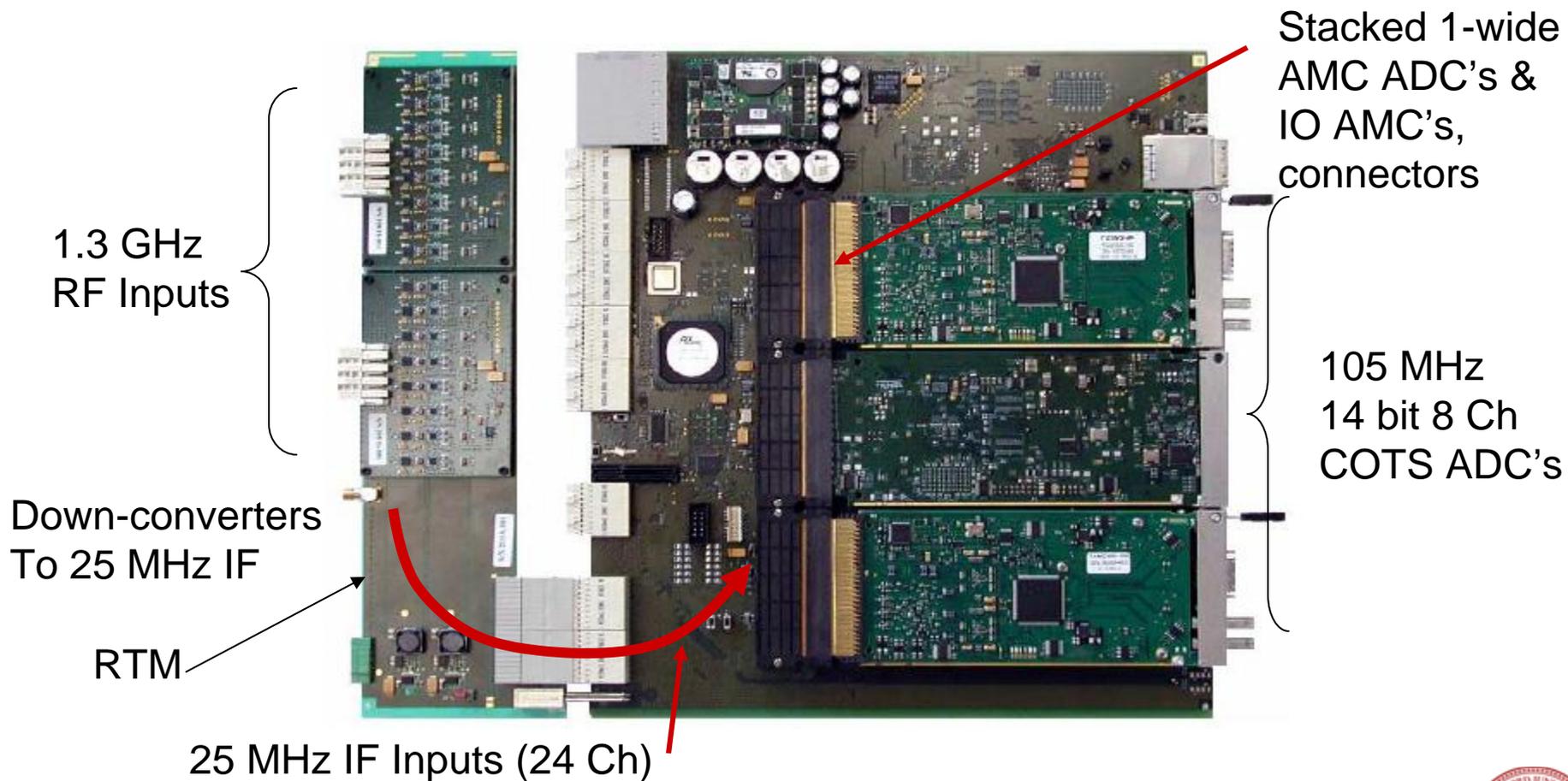
II. Accelerator Applications

DESY Prototyping

- ATCA Solution for 1.3 GHz LLRF (Simrock)
 - Controls 1 RF station, ~28 cavities
 - First prototype operational, 2nd starting
- MTCA Solution for 2.6, 3.9 GHz RF, RF station interlocks (Rehlich)
 - Prototyping phase in progress
 - Propose vendor supplied 12 ch fast ADC/DAC module for RF, fast interlocks

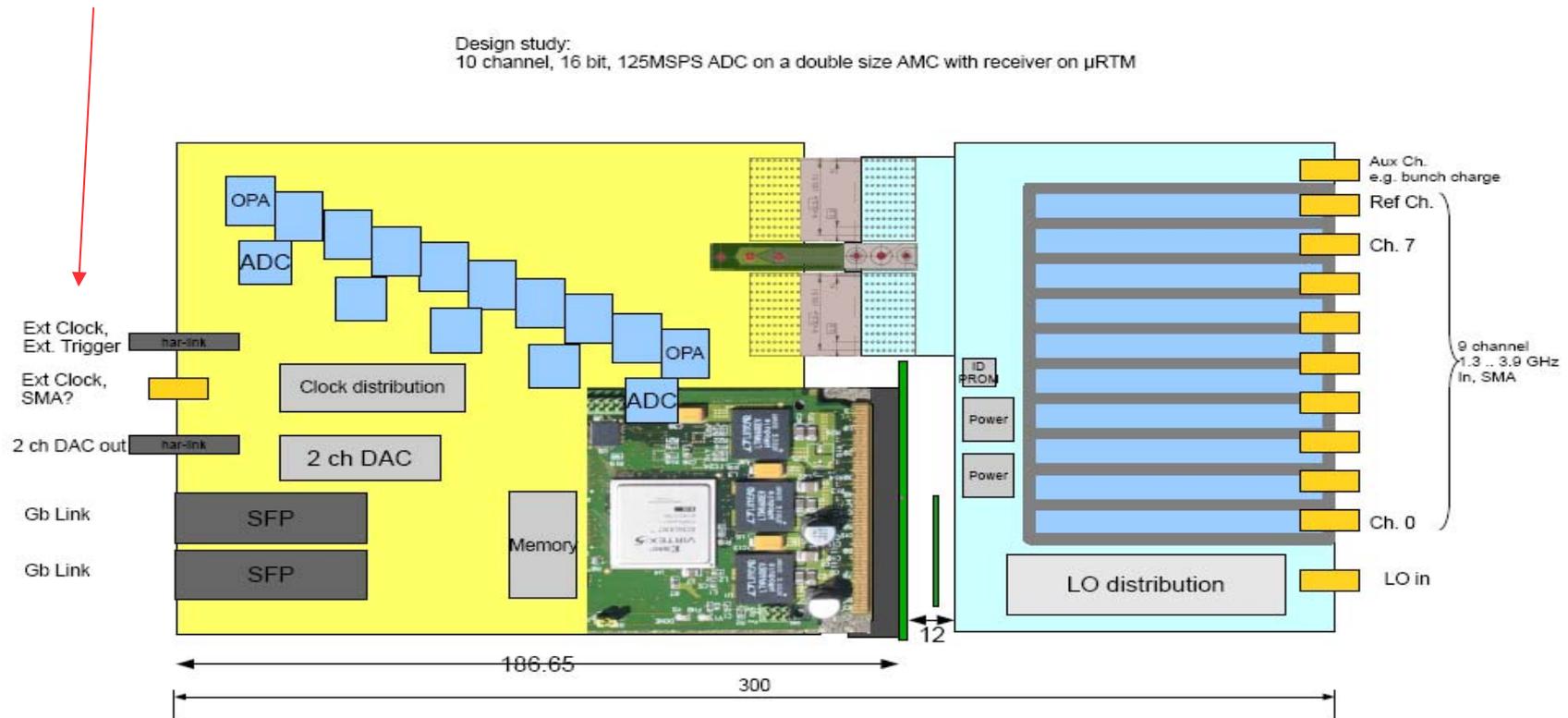
ATCA LLRF Prototype

ATCA-based LLRF control system



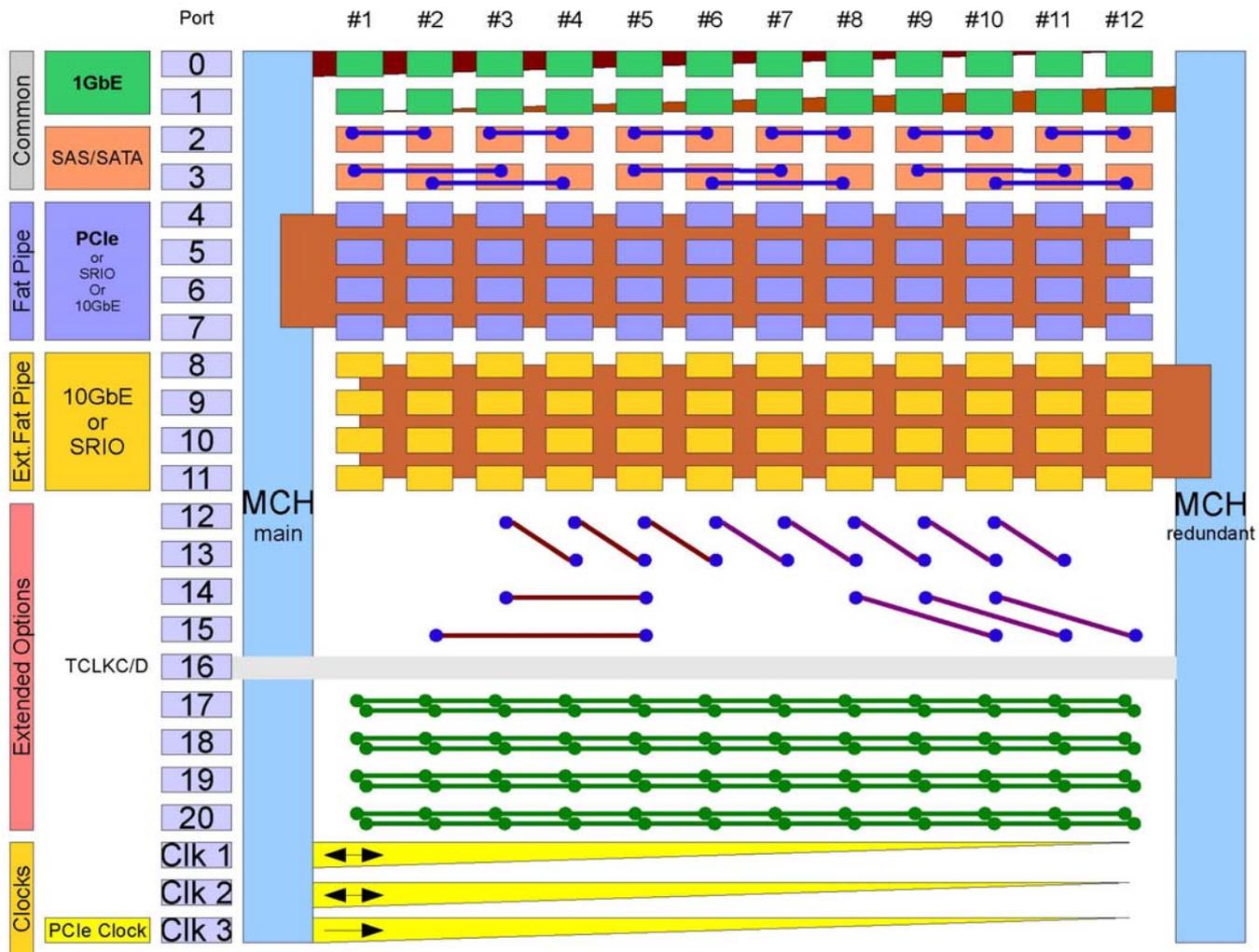
2-Wide AMC MTCA Design

Note – Clocks & triggers will be distributed via Timing module driving extended options region of AMC backplane (RL)



12 Channel 16-bit 125 MHz ADC Module on 2-wide AMC w/ Rear IO

Clocks & Triggers in MTCA



Courtesy K. Rehlich, DESY

Clock & Trigger Lines Allocation

Clocks and Triggers

- Low Jitter Clocks (Clk1 + Clk2):
 - Radial distribution from the MCH
 - Source can be one AMC (or external source)
 - PCIe Clock on CLK3
 - None Critical Clocks and Triggers:
 - M-LVDS bus lines
 - Terminated on both ends of the backplane
 - Source can be one AMC, receiver can be any AMC
- 2 high precision clocks + up to 8 clocks or triggers

GigaLink Connections

- Port 4-7 (MCH 1):
 - PCIe as the preferred I/O interface
 - Optional: SRIO or 10GbE (depends on MCH configuration)
- Port 8-11 (MCH 2 - redundant):
 - SRIO or 10GbE (depends on MCH configuration)
- Direct point-to-point links:
 - Use Port 2 – 3 (SAS/SATA) connections on none CPU AMCs
 - Use port 12 – 15 for additional connections

Can we find a 'standard' allocation of ports 12-15 that covers 90% of the use cases?

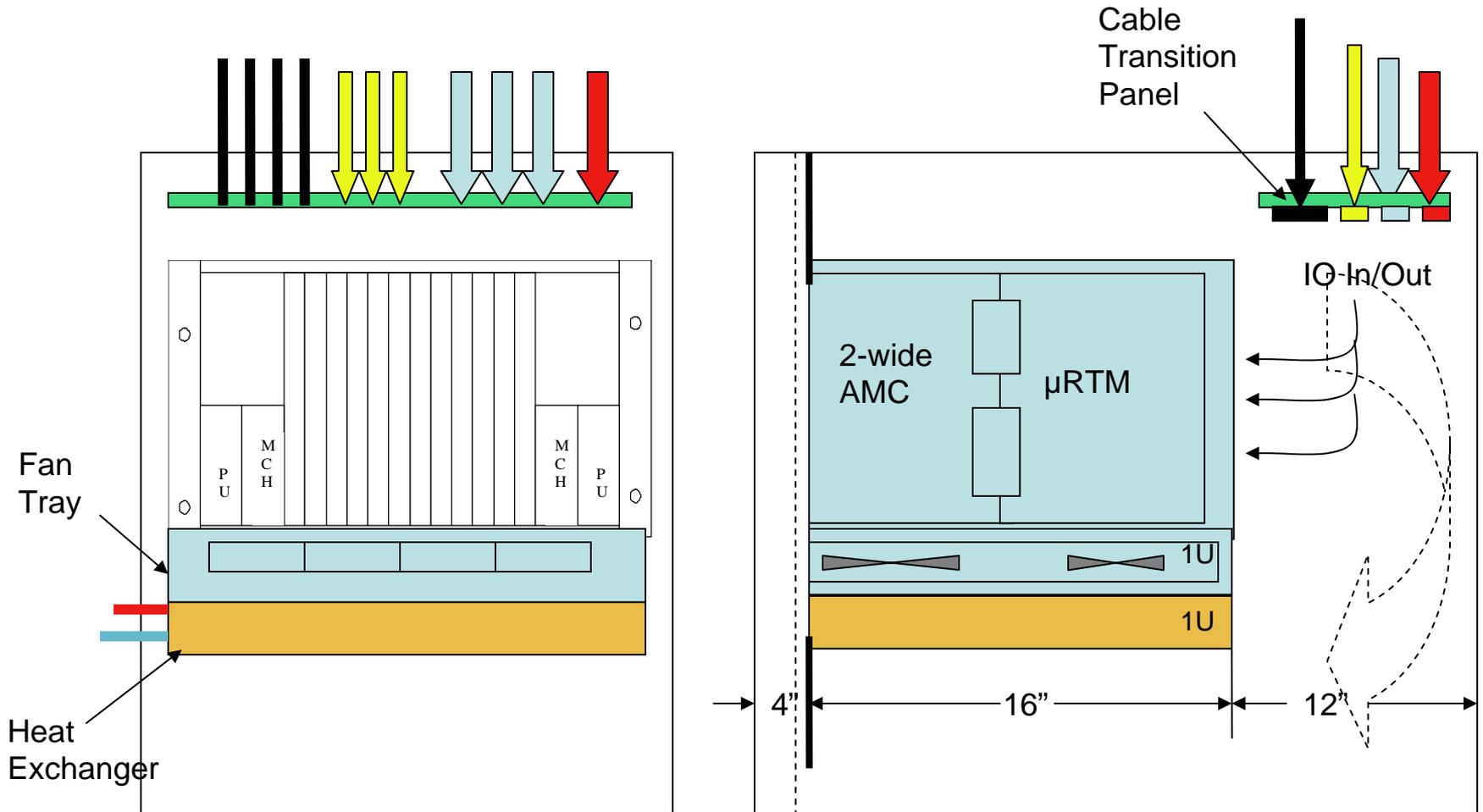
Interlocks etc.

- Provide 8 lines of M-LVDS (terminated) for general purpose use
- Possible applications:
 - Interlock wired-OR
 - Low quality clocks
 - Triggers
 - Other communications/signaling to all boards from one source on hardware level

SLAC Controls Upgrade

- Collaborating w/ DESY on MTCA approach
 - 80 RF stations S-Band 3.5 μ sec pulse (Phase1), 240 stations total
 - ADC-DAC, interlock requirements very similar
 - ~6 channels 25.5 MHz IF, 6 ch fast interlocks, 20 ch slow interlocks, 2 DAC channels controls
- Prototyping
 - Designing compact RF section to make crosstalk, temp sensitivity measurements LO/IF
 - Tested ERNI connector crosstalk – OK to >-90 dB using alternate channels
 - Making cooling stability measurements on existing PAD, mini-rack air-water cooled
 - Investigating interconnect concepts from log-hauls to RTM inputs
 - Requesting vendor quotes on packaged MTCA & Mini-Rack

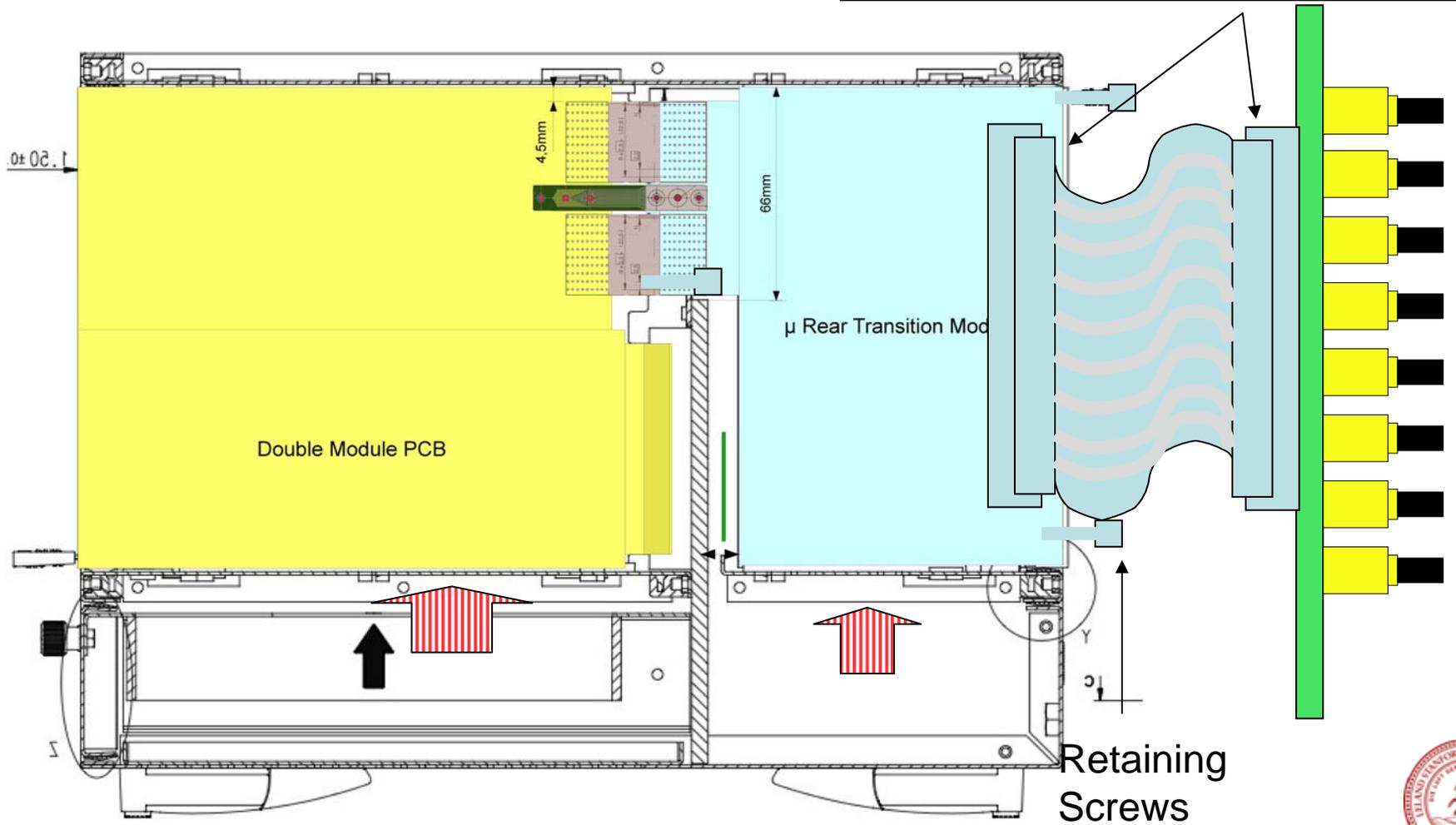
MTCA Mini-Rack Proposal - SLAC



Side View in Schroff Prototype Shelf

RF Input Example

8 Ch Coax Subminax Plugs
(e.g. Harting or SMA)



Accelerator Applications Summary

- Lab collaboration with industry working well
- New DESY, SLAC projects helping define, drive requirements
- Discussions held with ITER on possible uses of ATCA (JET already using for fast plasma control)
- Potential benefits of collaboration: Save duplicating engineering effort; achieve better industry support; open source solutions for both HW, SW.