Fermilab

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PXIE LLRF Status

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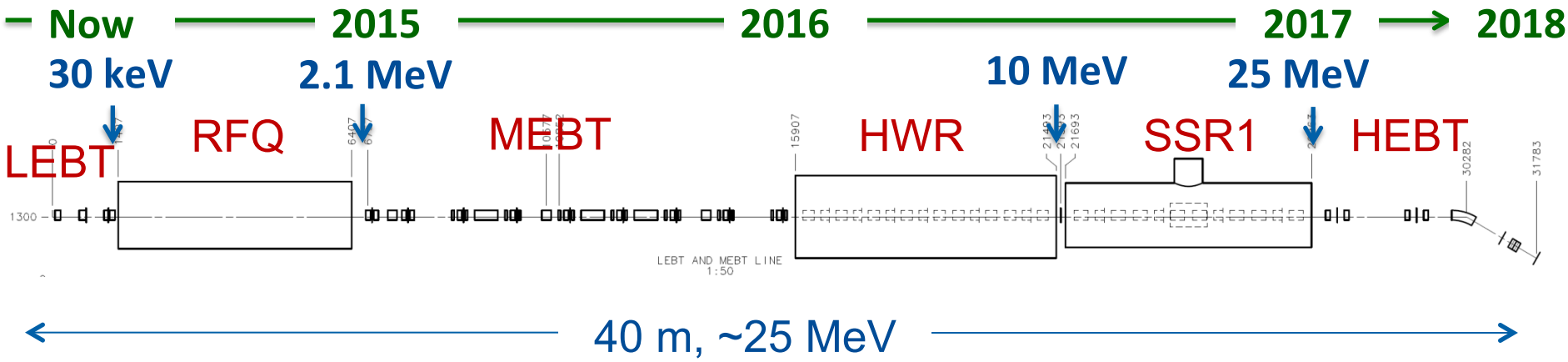
PXIE Low Level RF Group Involvement



PXIE will address the address/measure the following:

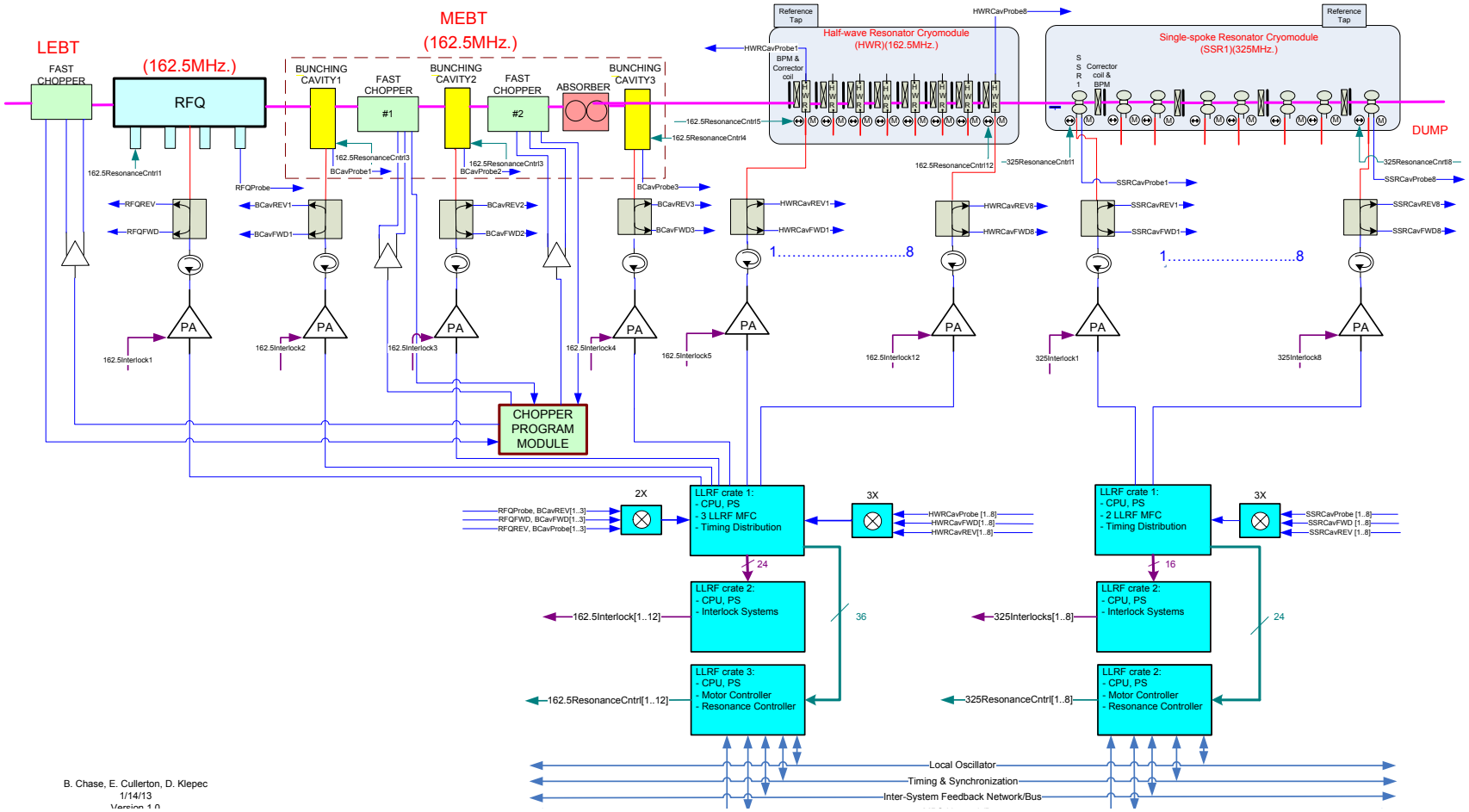
- LEBT pre-chopping
- Vacuum management in the LEBT/RFQ region
- Validation of chopper performance
- Bunch extinction
- MEBT beam absorber
- MEBT vacuum management
- Operation of HWR in close proximity to 10 kW absorber
- Operation of SSR with beam, including resonance control and LFD compensation in pulsed operations
- Emittance preservation and beam halo formation through the front end

Collaborators
- ANL: HWR
- LBNL:LEBT, RFQ
- SNS: LEBT
- BARC: MEBT, SSR1

LLRF Systems needed to meet R&D Goals

- 325 MHz Horizontal test stand
  - Support for CW and pulsed mode operation
  - Operational now with some upgrades planed
- 650 MHz Horizontal test stand
  - Support for CW and pulsed mode operation
  - Supplied by India Q3FY16
- PXIE
  - Master Oscillator and Phase Reference distribution line
    - 162.5 MHz & 325 MHz (In construction phase)
  - RFQ – 162.5 MHz (Q4FY15)
    - 2 RF amplifier system
  - Buncher - 3 cavities - 162.5 MHz (FY15)
  - Half Wave Resonators - 8 cavities @162.5 MHz (FY17)
  - SSR1 - 8 cavities @ 325 MHz (FY17)
  - Kicker waveform generator

PIXIE RF Stations Diagram



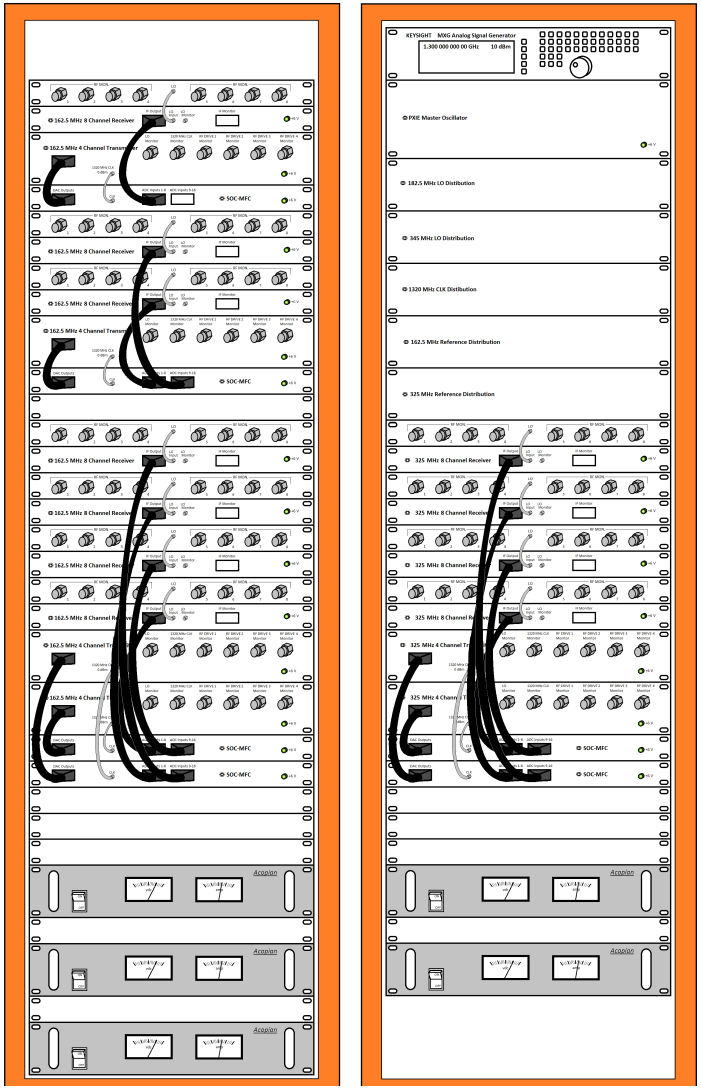
PXIE LLRF Rack Front and Rear View

Fermilab PXIE LLRF Racks

RFQ

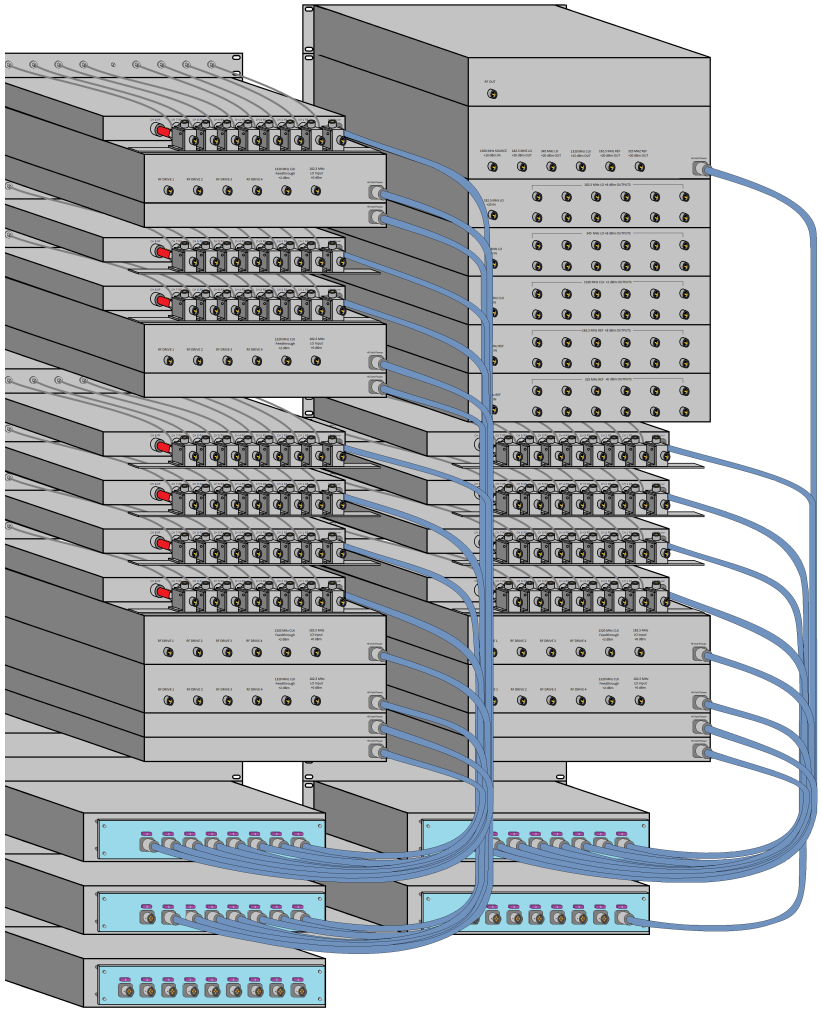
3 x Buncher

Half Wave Resonators

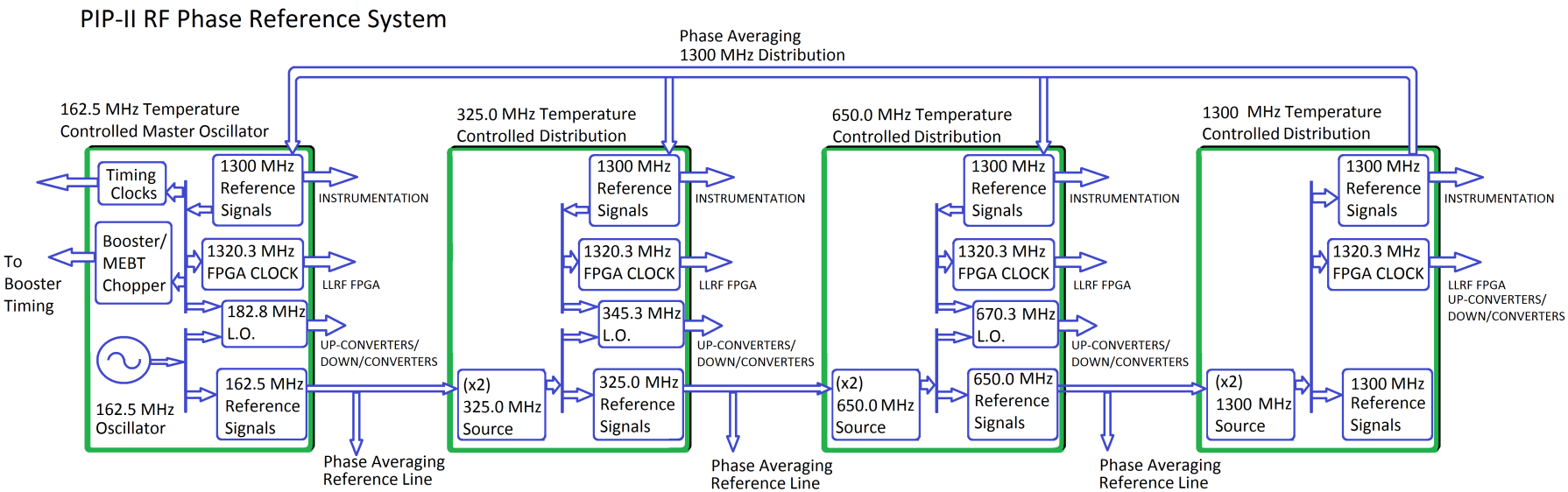


SSR1 Cryomodule

PXIE LLRF Racks



Phase Reference Lines (162.5, 325, 650 ,1300 MHz)



Multi-frequency Phase References and Local Oscillators

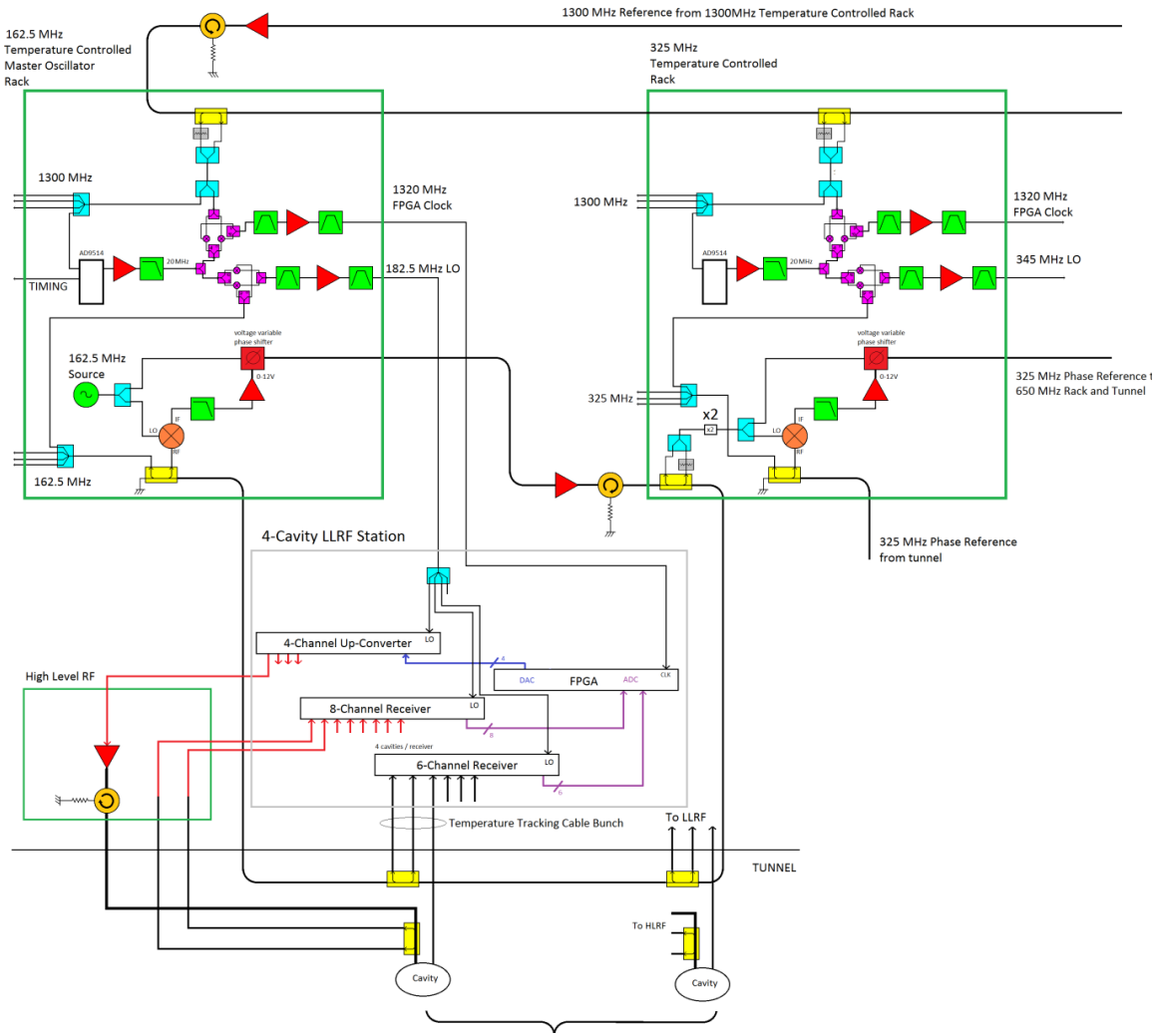
We are building up the first sections for PXIE

Details of First 162.5 MHz RF Section

Phase stability across harmonics (400 fs)

Temperature controlled racks and component plates

We have this experience and see a path forward

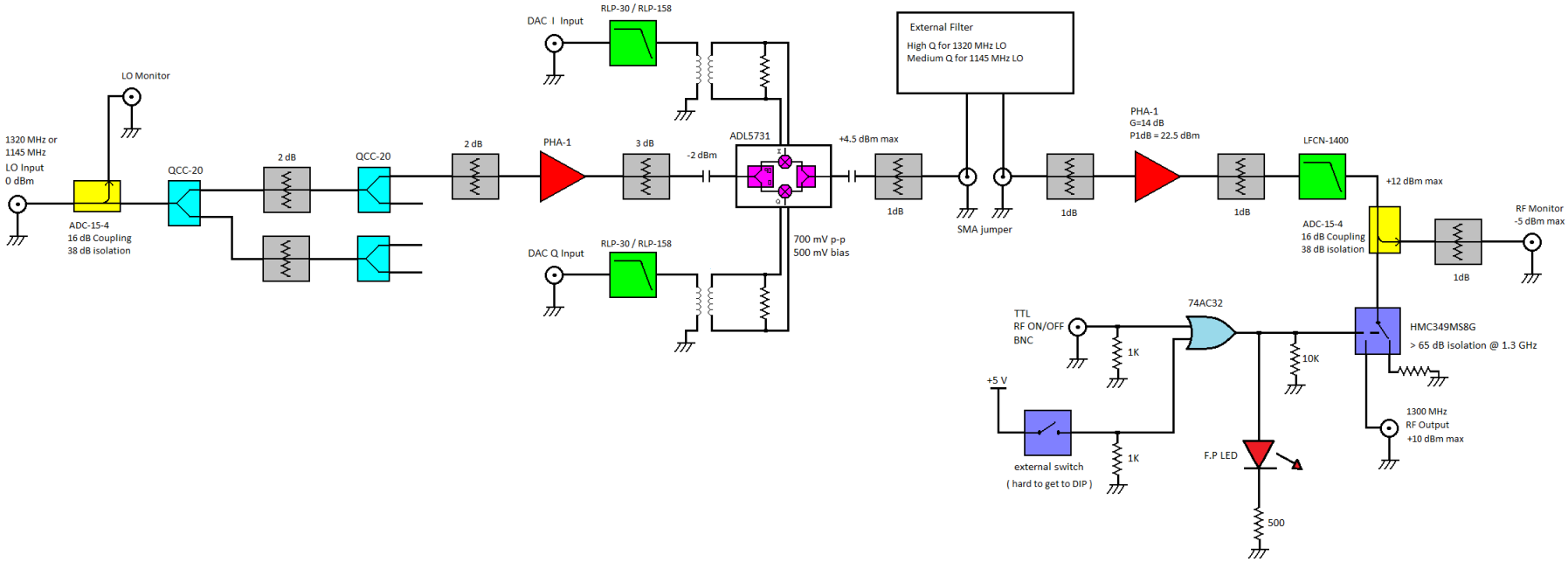


162.5 MHz 8 Channel Receiver

One module is complete and we have parts for a second

Up-converter diagram (1 of 4 channels in module)

In design phase for
162.5 MHz and 325 MHz



MFC First Generation Board

This will be used for the RFQ in the near future

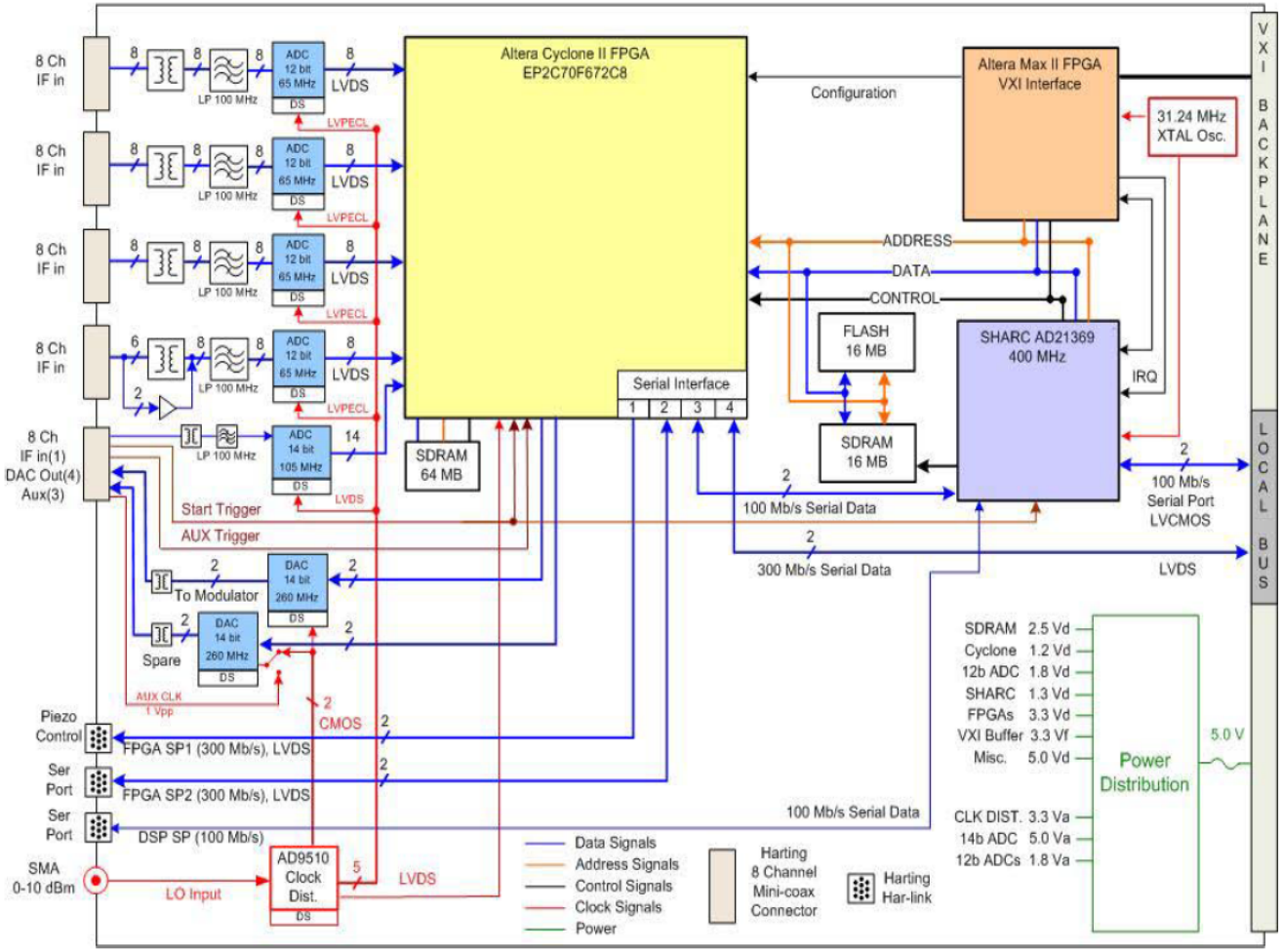


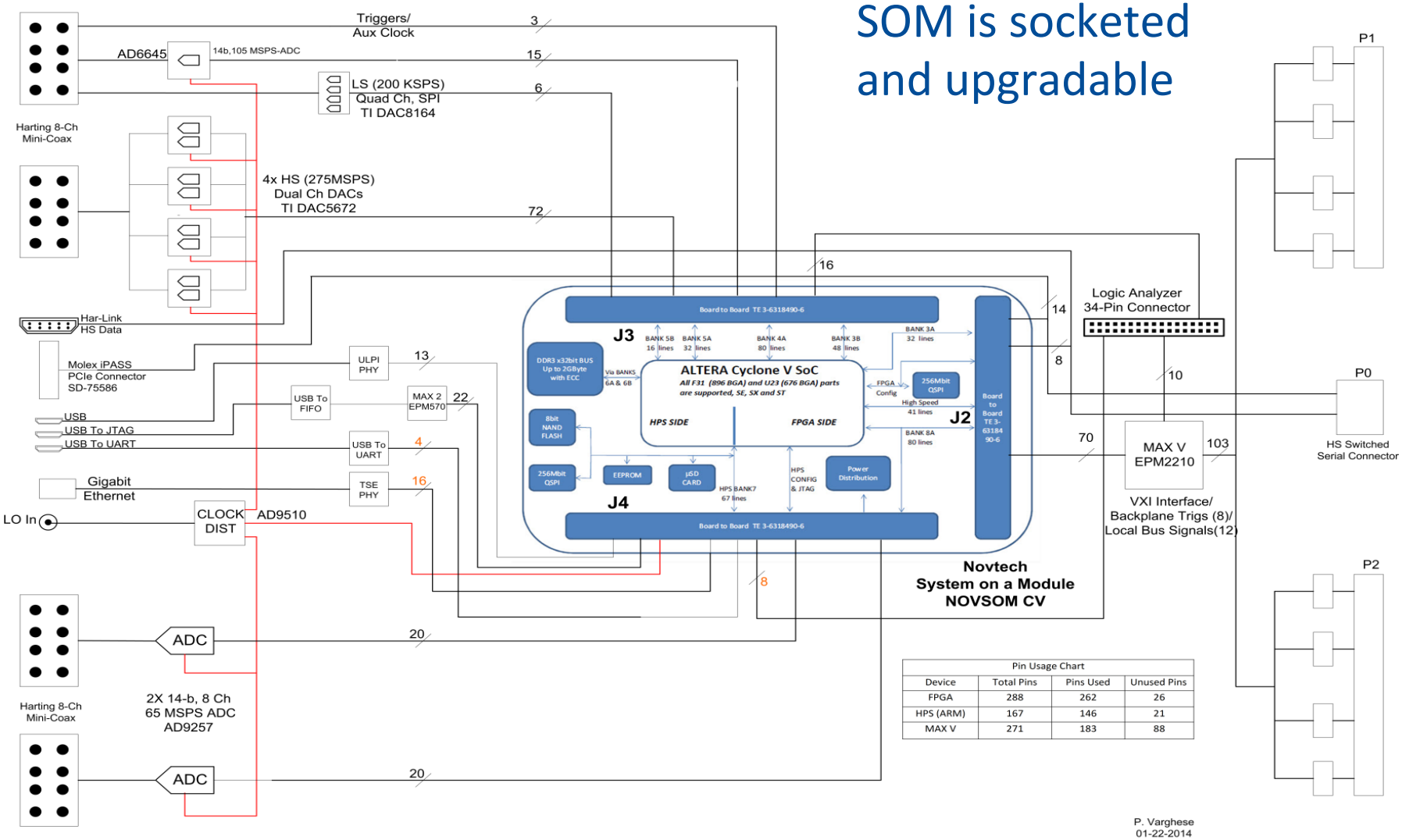
Figure 1: MFC Board Overview

MULTICHANNEL VECTOR FIELD CONTROL MODULE FOR LLRF CONTROL OF SUPERCONDUCTING CAVITIES*

P.Varghese#, B. Chase, B. Barnes, J. Branlard, P.W. Joireman, D. Klepec, U. Mavric, V. Tupikov
Fermilab, Batavia, IL 60510, U.S.A.

System on Module Multi-cavity Field Controller (SOM-MFC)

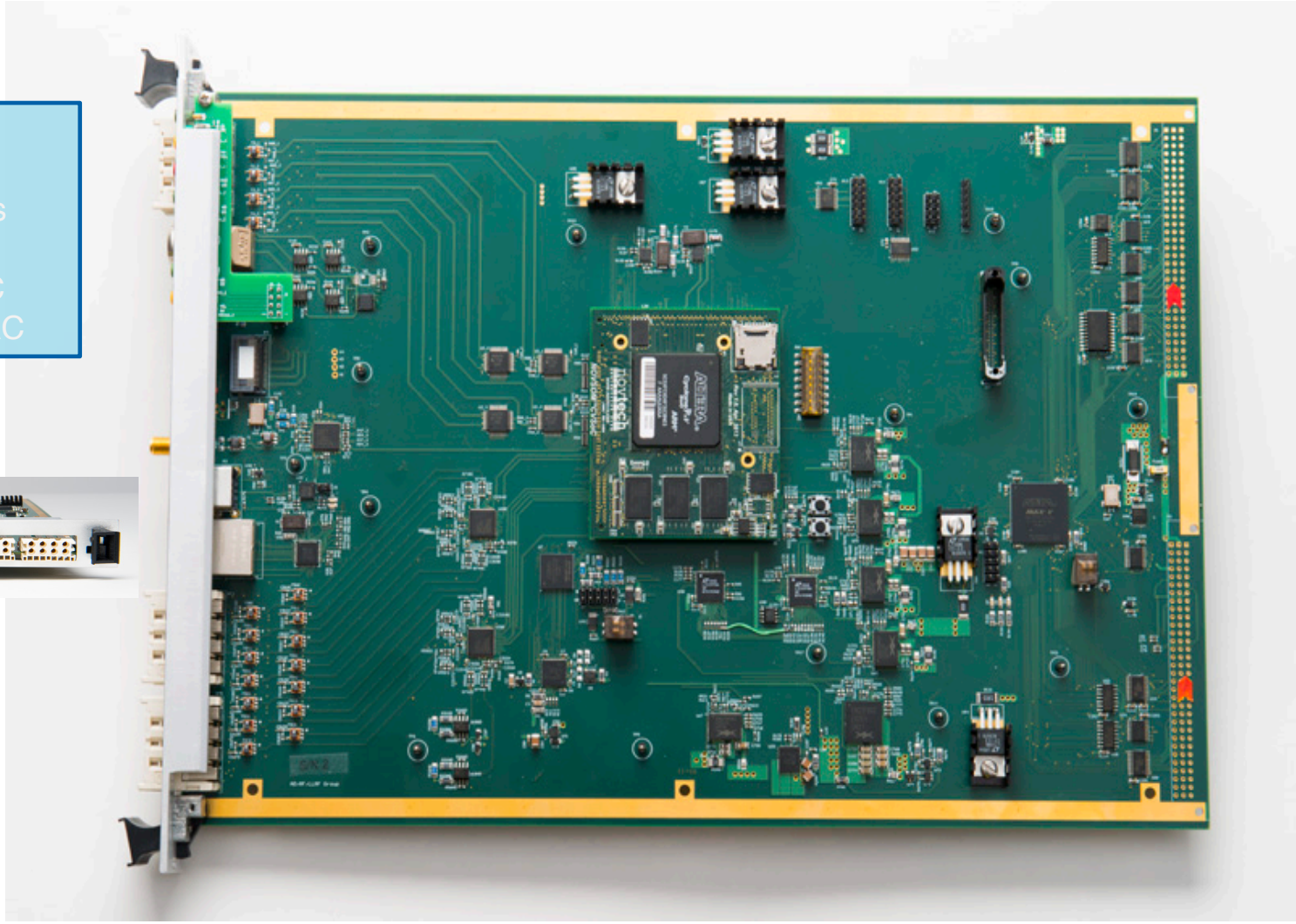
SOM is socketed and upgradable



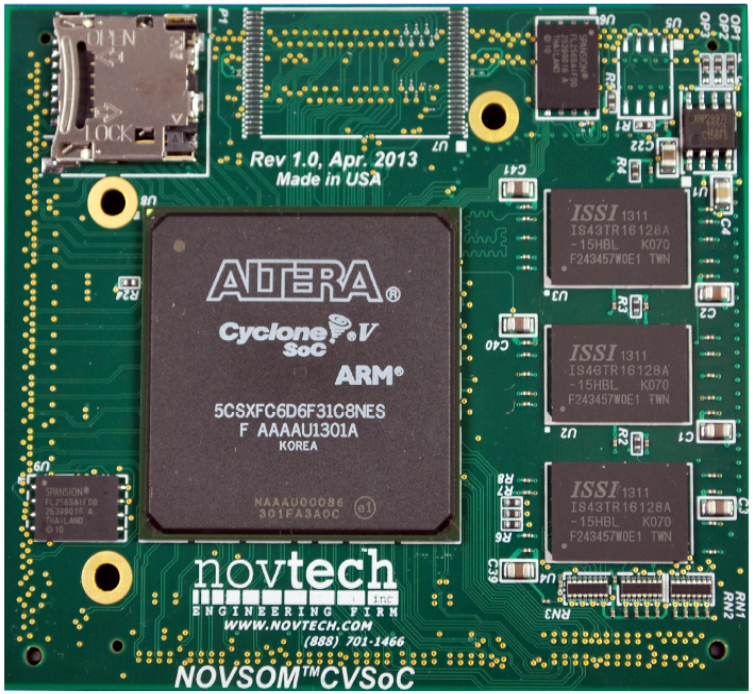
Pin Usage Chart			
Device	Total Pins	Pins Used	Unused Pins
FPGA	288	262	26
HPS (ARM)	167	146	21
MAX V	271	183	88

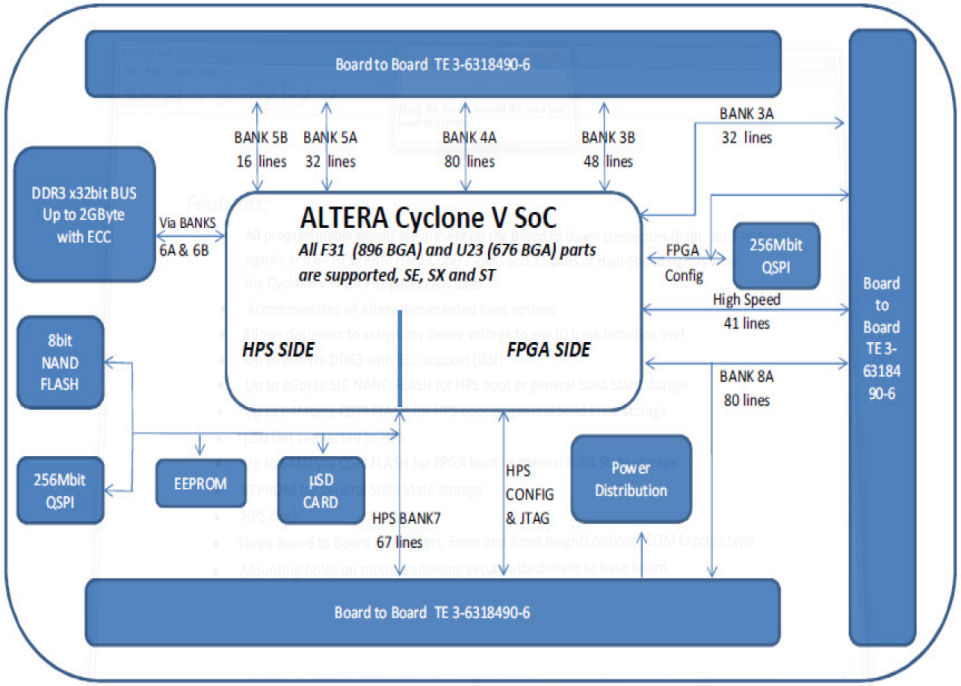
SOC-MFC Second Generation Board

Features
- 16 ch ADC, 8 DAC
- High-speed data bus (PCIe)
- 14-bit, 65 Msps ADC
- 14-bit, 275 Msps DAC



MFC Second Generation Board
NOV SoM (System-on-Module)



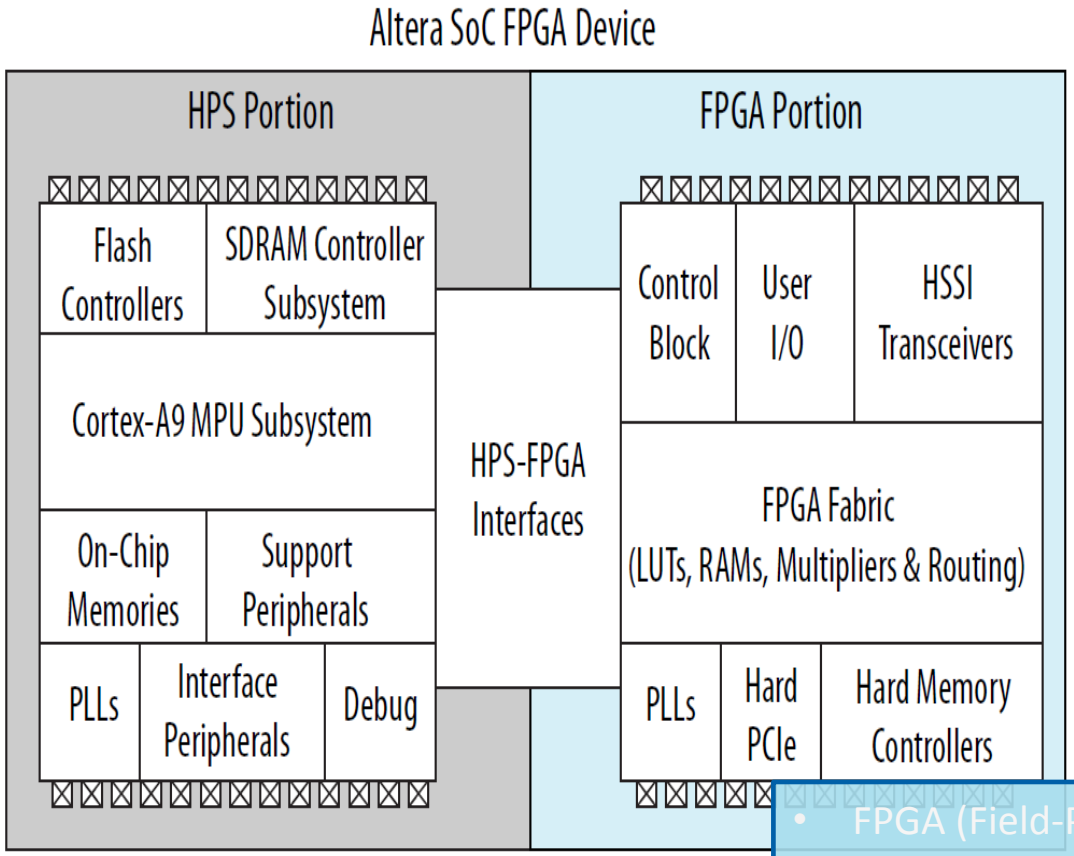


Plug-in module allows easy system upgrade

Delivery is 10 weeks late - problems communicating with memory

NOVSOM CV Product Brief

Controller Overview



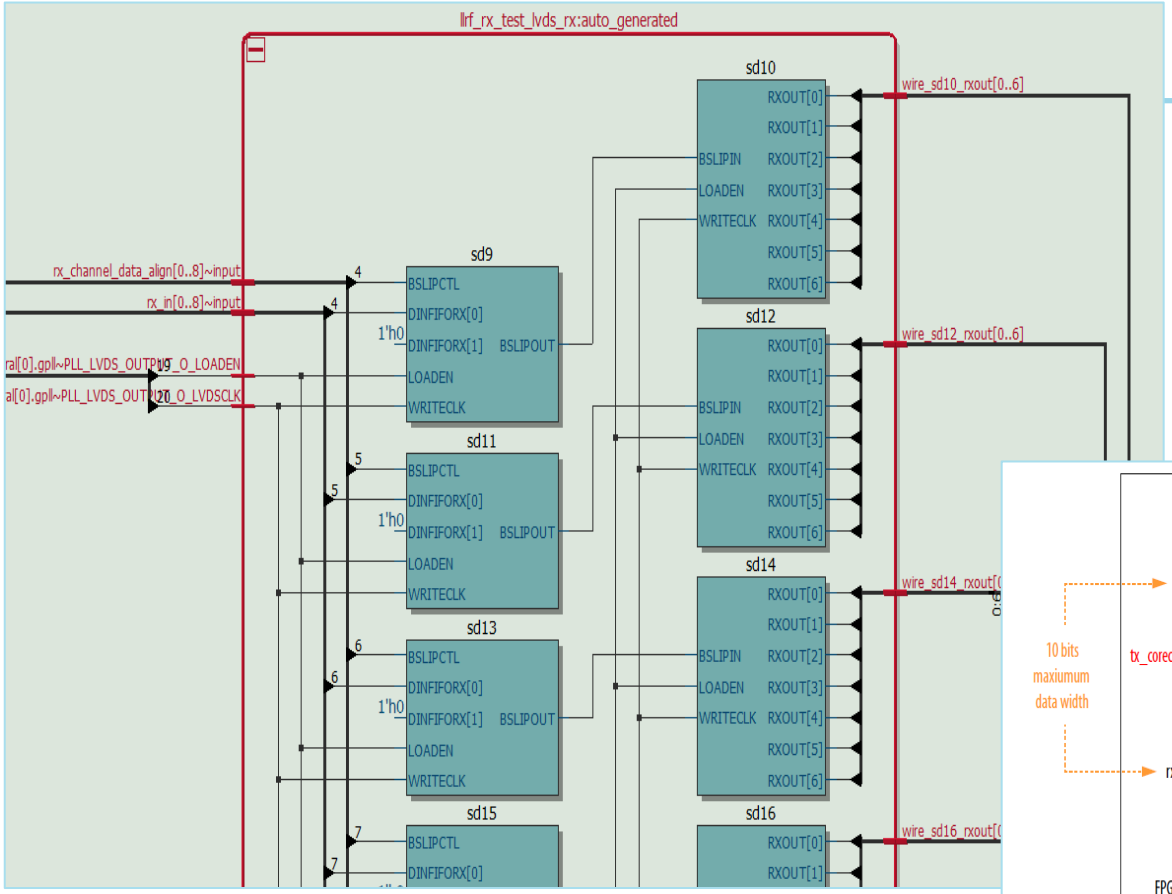
- FPGA (Field-Programmable Gate Array)
  - 670 MHz Max Input Clock
  - 875 Mbps Max RX LVDS
  - 550 MHz Max Internal Operating Frequency
- HPS (Hard Processor System)
  - Dual-core ARM Cortex-9
  - 925 MHz Max Core Frequency
  - 400 MHz Max Interconnect Frequency

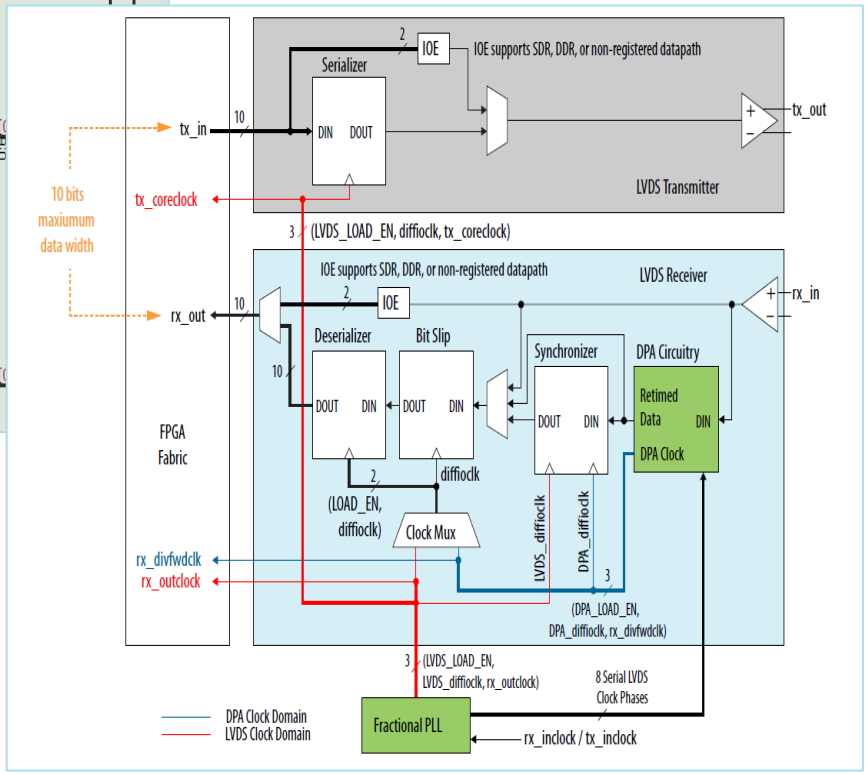
A decent linux computer with direct interface to a high performance FPGA

Altera, Cyclone V Design Handbook
Altera, Cyclone V Device Datasheet

High-Speed Signalling

This is a current point of struggle

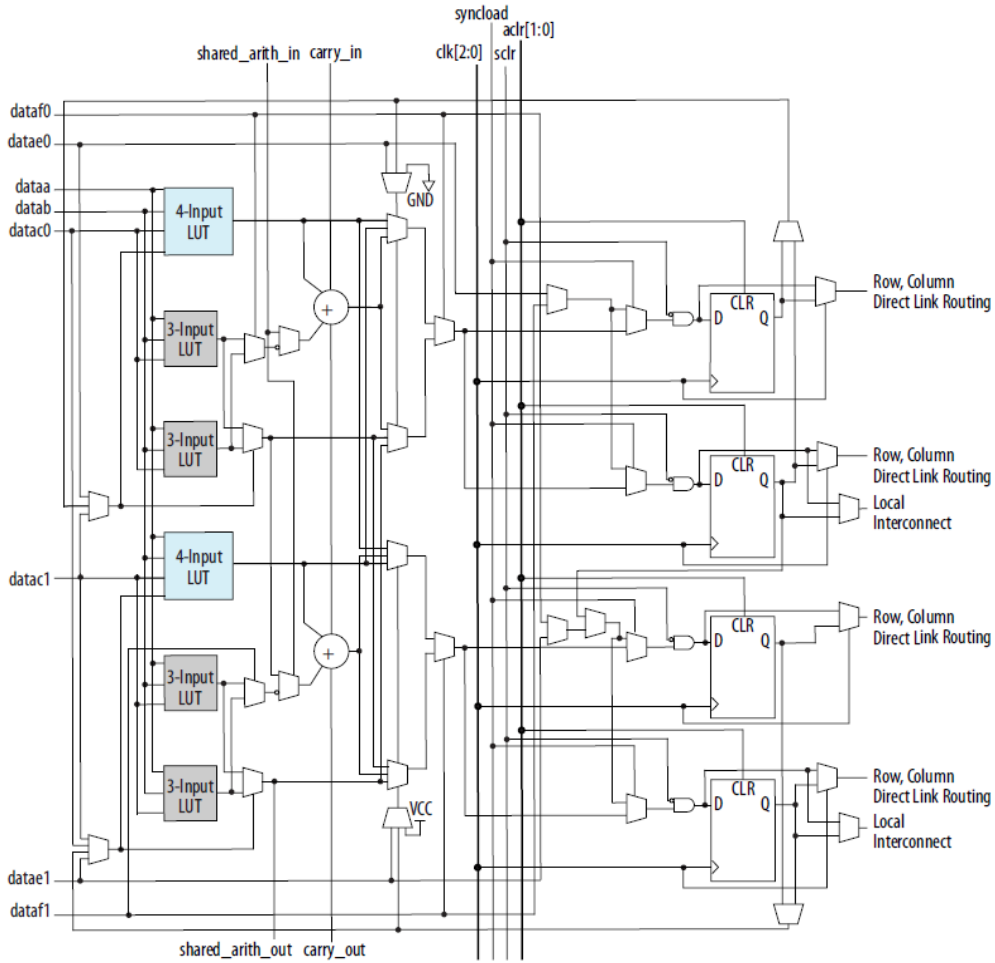




- Use of dedicated Serializer/Deserializer hardware for high-speed data
- Limited number of channels per device
  - Requires layout and planning reviews and expertise

Altera, Arria V Device Datasheet
Altera, Quartus II 14.1

FPGA Basic Logic Unit



Altera, Cyclone V Design Handbook
Altera, Cyclone V Device Datasheet

Controller Implementation(example)

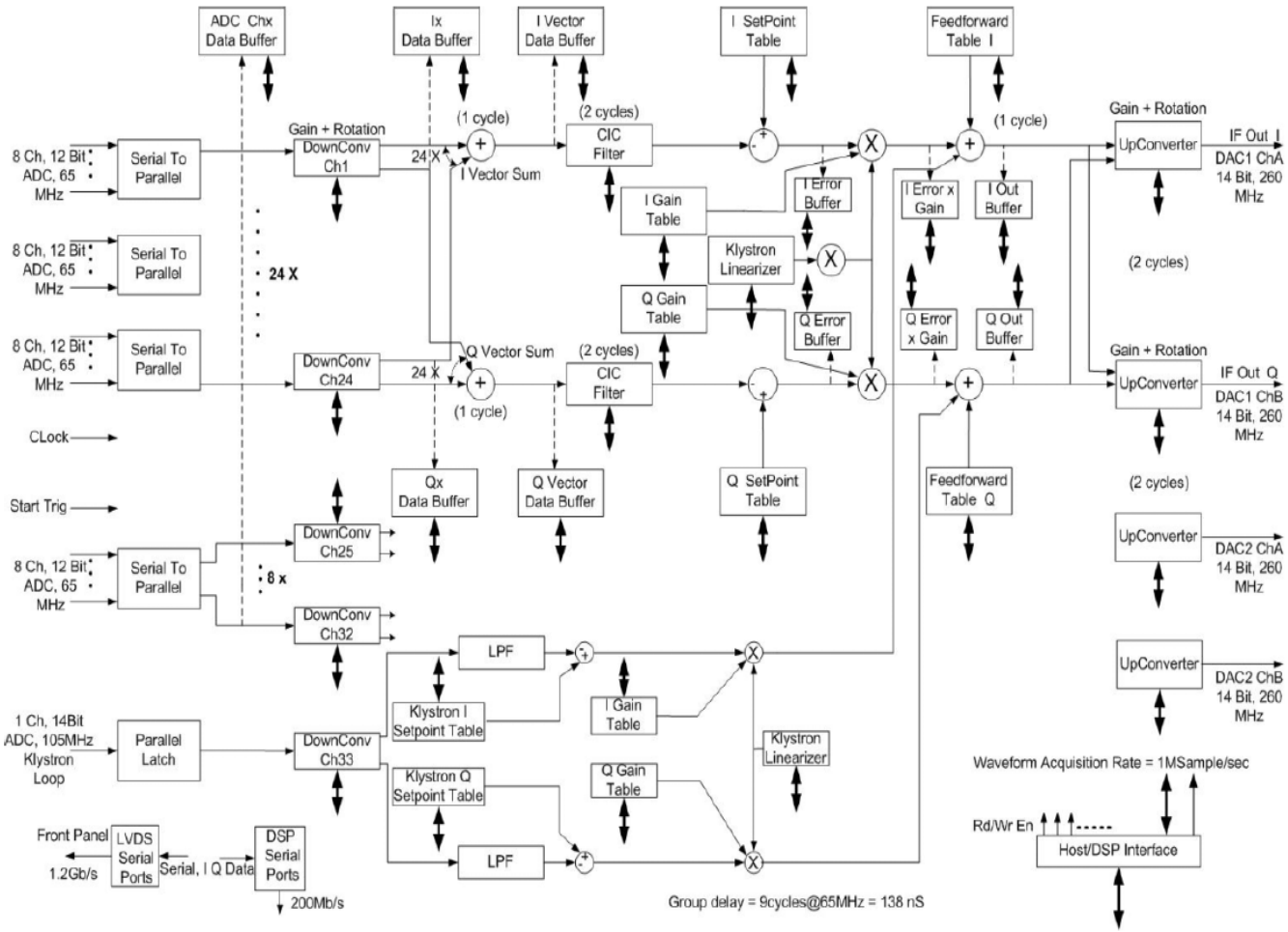
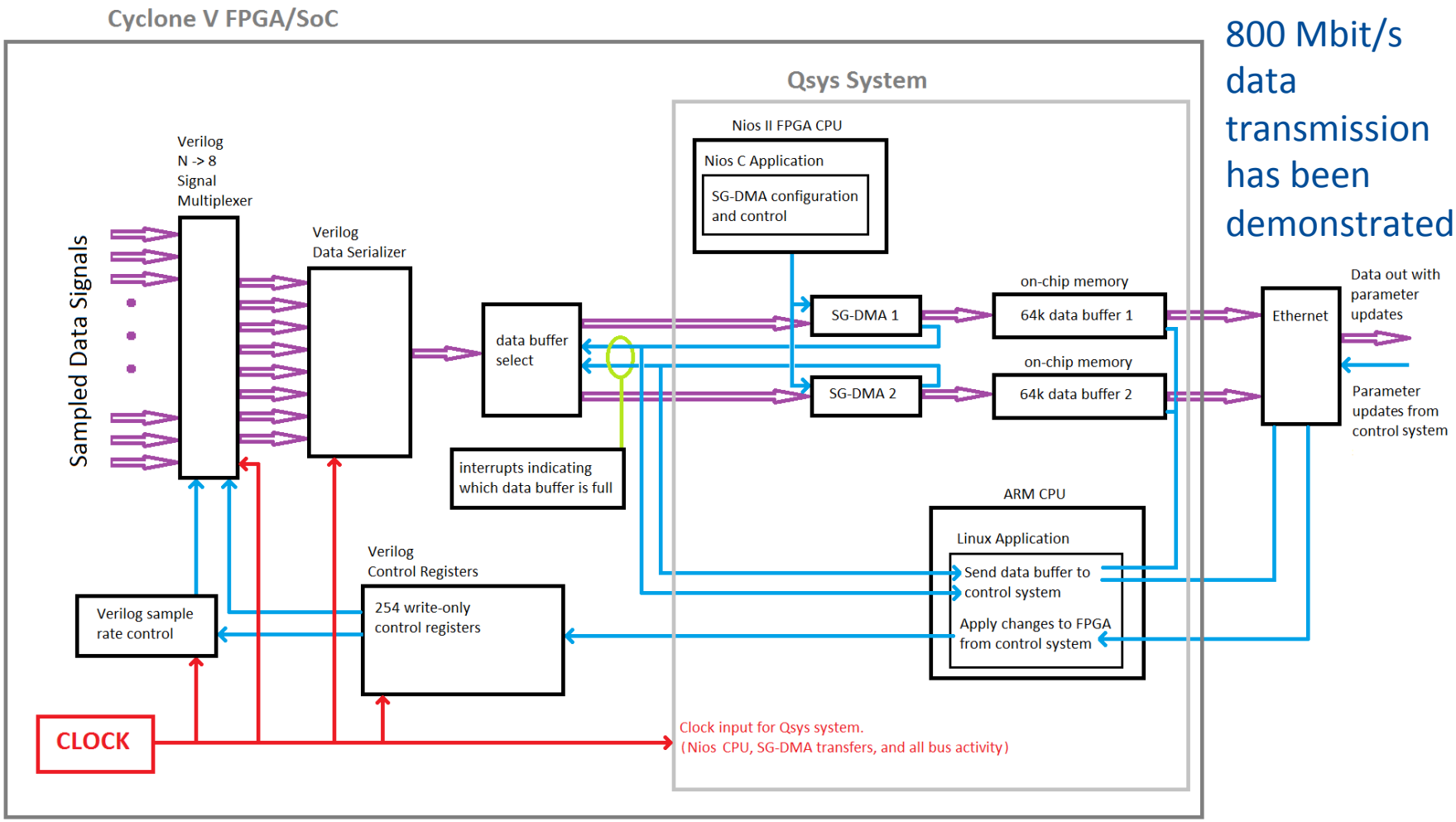


Figure2: FPGA Signal Processing

P.Varghese#, B. Chase, B. Barnes, J. Branlard, P.W. Joireman, D. Klepec, U. Mavric, V. Tupikov
Fermilab, Batavia, IL 60510, U.S.A.

SOC Data Acquisition Software / Firmware Model



800 Mbit/s data transmission has been demonstrated

Features that take time

- System Timing and performance Characteristics (Systick)
- Device Reconfiguration and Management
- Interrupt Management
- Intelligent Clocking
- Hardware Feature Limitations
- Embedded vs Firmware vs Front-end Code

Resonance Control
Piezo amplifier specifications

- 8 independent low noise piezo amplifiers to cover 4 cavities
  - 4 spare amps that may be ganged for additional current
- 0-100V differential output (50 V to ground)
  - Rear panel twist lock 4 wire SpeakOn connector
- 100 mA peak, 78 mA RMS continuous drive current per amp
- DACs driven over SPI with 18 or 20 bit precision
- Noise floor of amp 26 uV RMS 0.03 Hz to 1 MHz
- Noise floor of DAC is 7.5 nV/Hz
- Drive V, output V and current for both legs monitored by 18 bit ADC
  - Analog control and monitor through front panel TRS jacks
- Independent channel enables via remote or local dip switch
- + - 16 V power supply
- temperature readback, module ID
-

PiezoDrive PDu150 three channel Ultra-low noise piezo driver

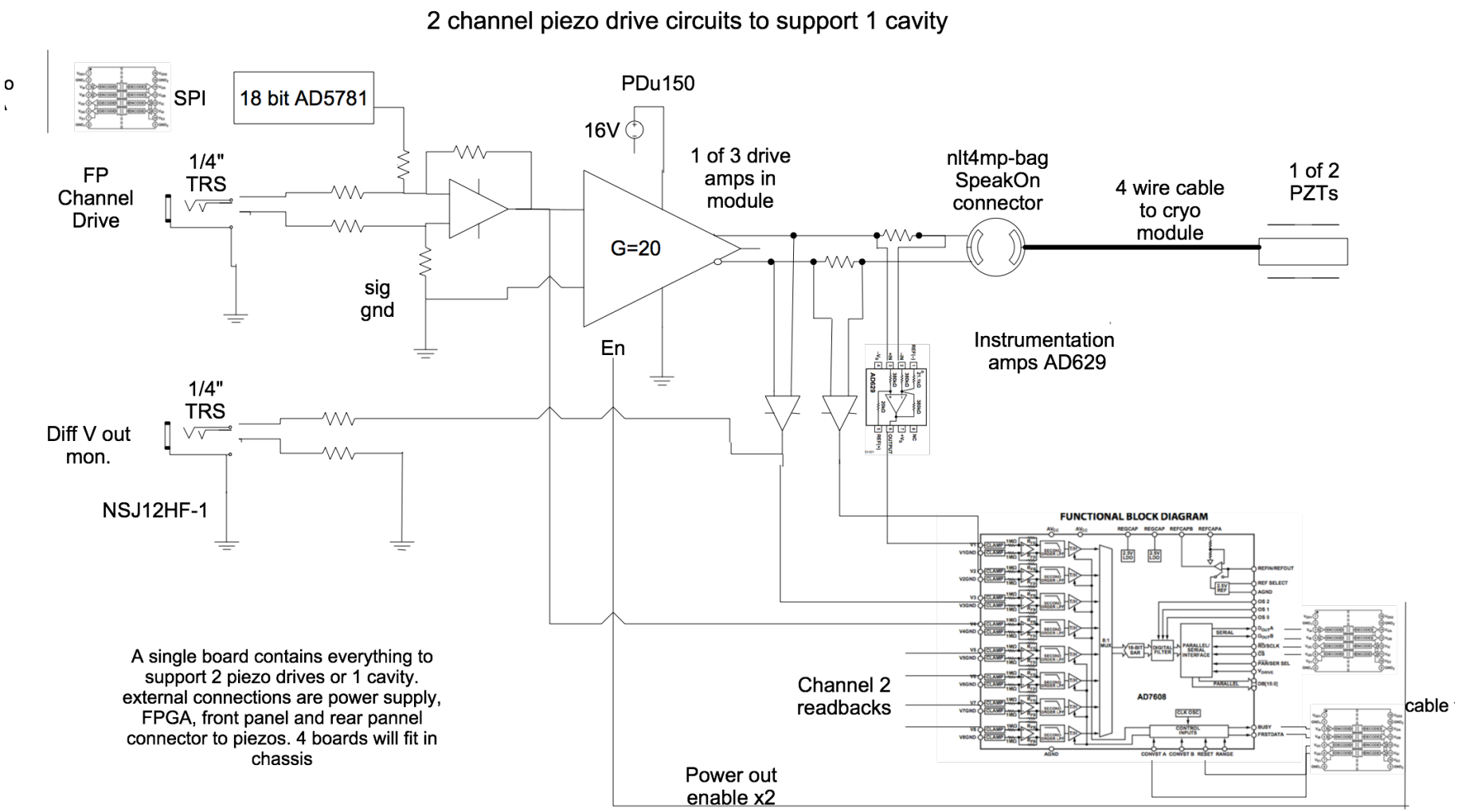
Specifications

Load Cap.	Bandwidth
No Load	180 kHz
10 nF	105 kHz
30 nF	40 kHz
100 nF	11 kHz
300 nF	3.8 kHz
1 uF	1.0 kHz
3 uF	320 Hz
10 uF	62 Hz
30 uF	24 Hz

Small signal bandwidth versus load capacitance (-3dB)

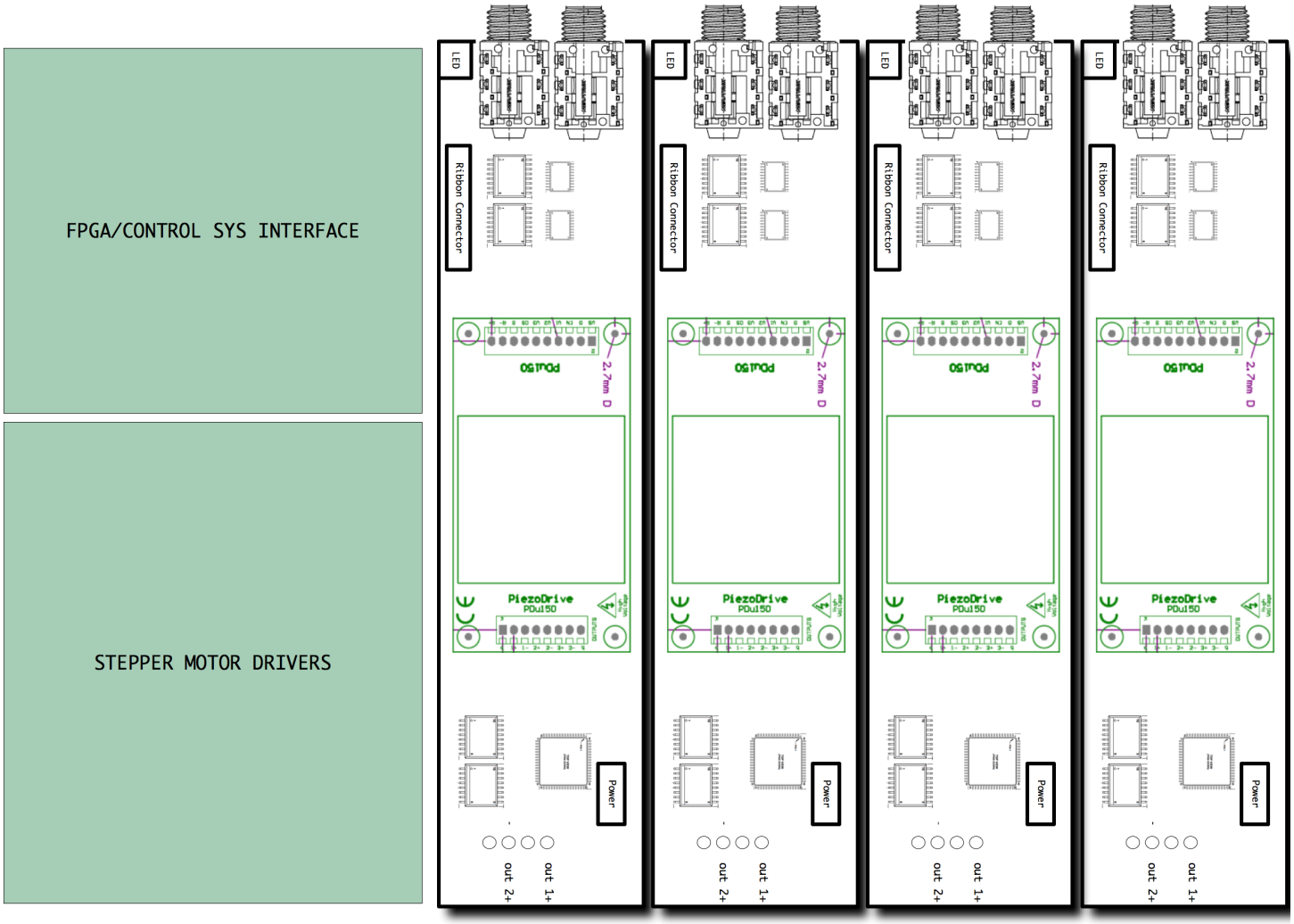
Specifications	
Power Supply	+24 V, Ground
Output Voltage	-30 V to +150 V
Peak Current	100 mA (300 mA single channel)
RMS Current	78 mA (235 mA single channel)
Power Bandwidth	80 kHz (150 Vp-p)
Signal Bandwidth	180 kHz
Slew Rate	38 V/us
Gain	20 V/V
Input Impedance	110 kOhm (Input), 3.3 kOhm (Offset)
Input Offset	+/- 5 mV
Load	Unlimited
Output Noise	26 uV RMS (1 uF load, 0.03 Hz to 1 MHz)
Protection	Short circuit, over-current, and temperature
Quiescent Current	100 mA (10 mA in shutdown)
Connectors	Screw terminals (AWG 20-30)
Dimensions	76 x 40 x 37 mm (L x W x H)
Environment	-40C to 60C (-40F to 140F)
Weight	80 gram

Drive module diagram



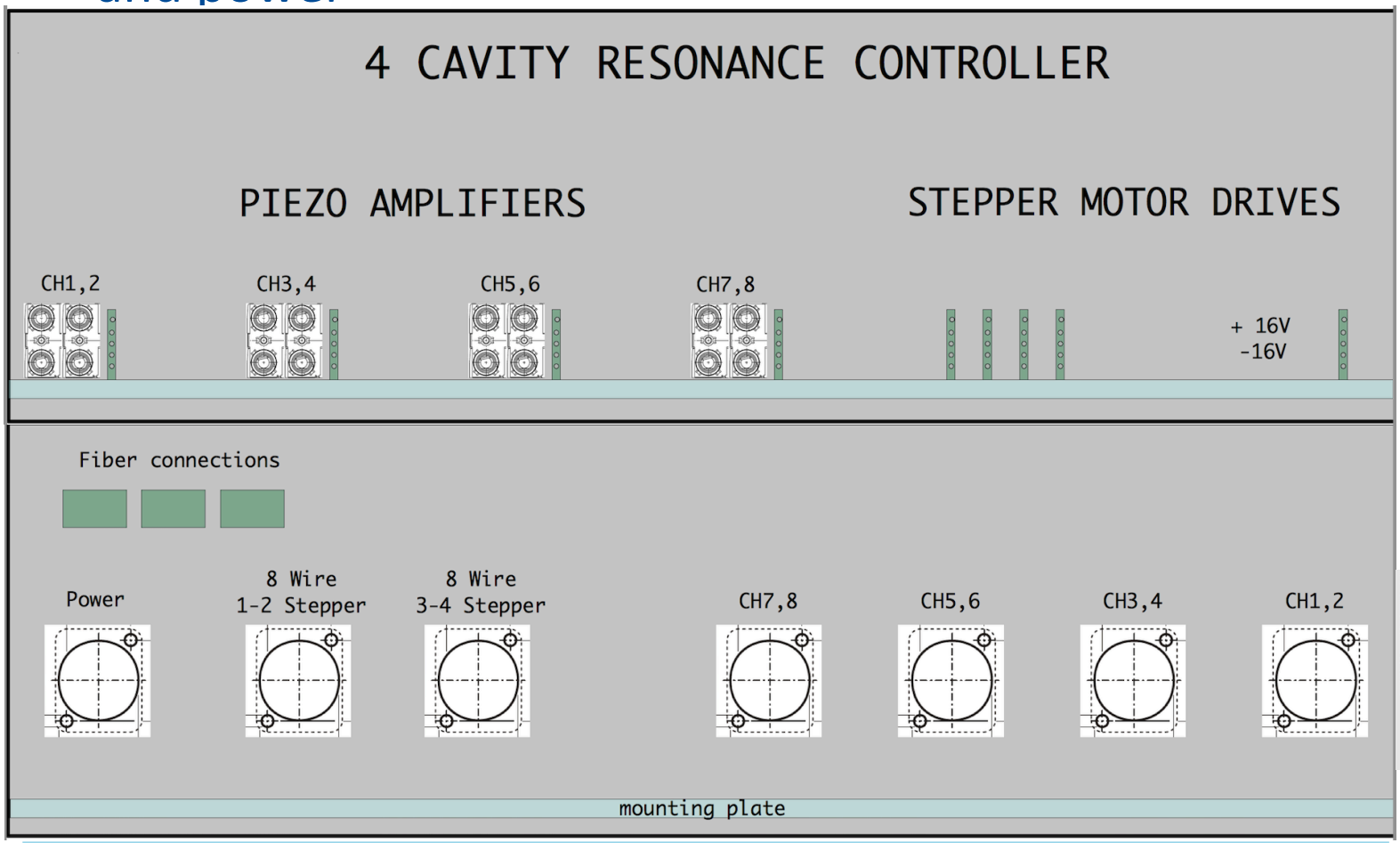
A single board contains everything to support 2 piezo drives or 1 cavity. external connections are power supply, FPGA, front panel and rear pannel connector to piezos. 4 boards will fit in chassis

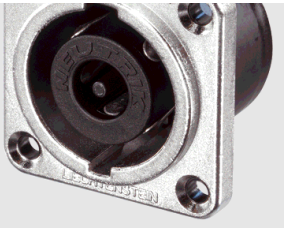
Resonance control chassis layout



Resonance control chassis

Nutrik connectors for piezo, stepper and power





Meeting FY15 PXIE goals

- 162.5 MHz down-converter will be completed soon
- Up-converter in the design stage
  - need addition funds to build
- Basic design of Master Oscillator and LO distribution is complete
  - many parts in-house, synthesizer on order
  - need addition funds to build
- SOC-MFC is behind by several months due to design issues and vendor delivery
  - need addition funds to build
  - Will bring up RFQ with first generation MFC
- Software and firmware have several months of work remaining