

200 Ω Chopper System Progress

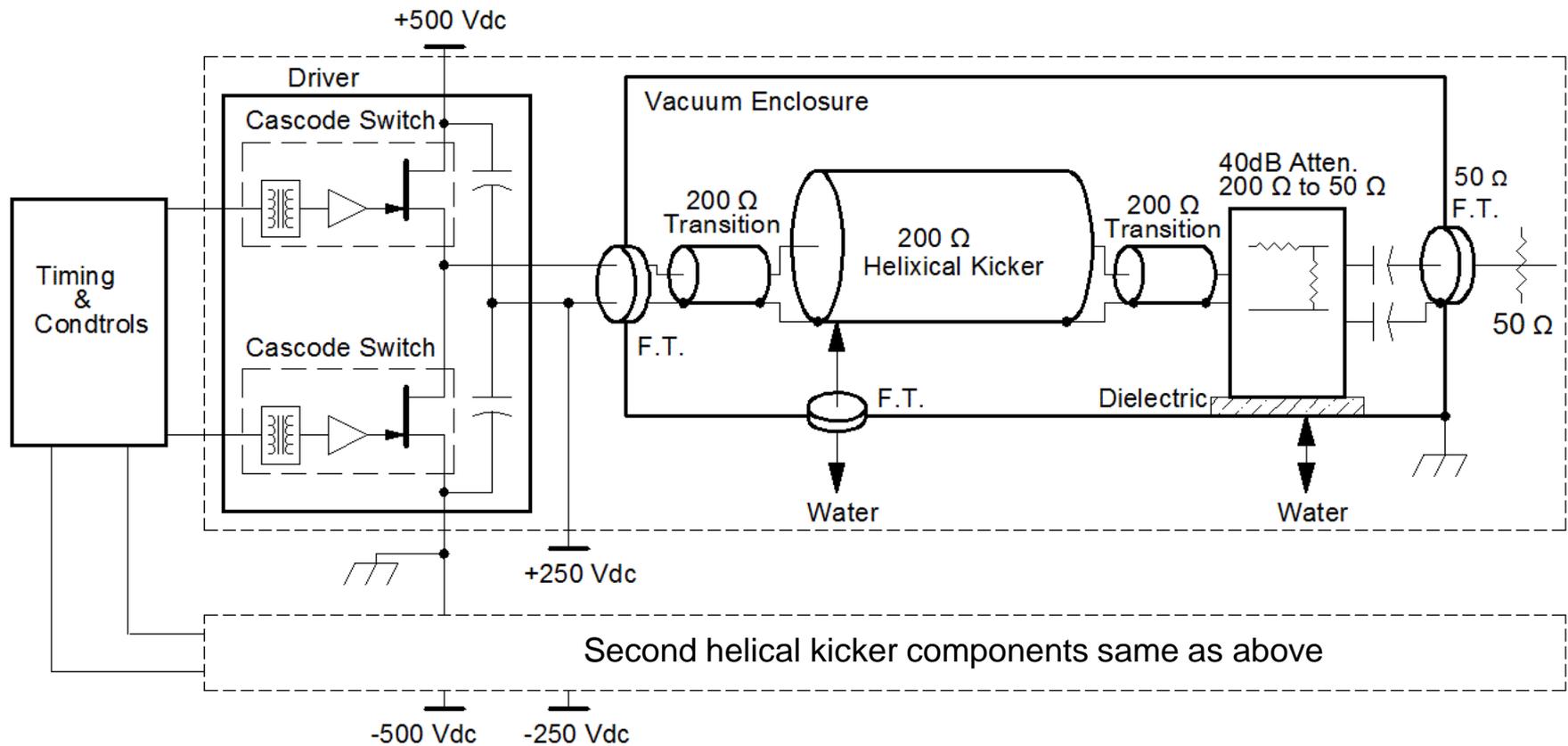
G. Saewert
Project X meeting
July 10, 2012



- Review of 200 Ω chopper system
- Helix modeling
- Reflection tests
 - 200 Ω load
 - 200 Ω transition lines
- Bipolar switch development
 - Drive signal isolation



Two helical kickers: their interconnections and biasing



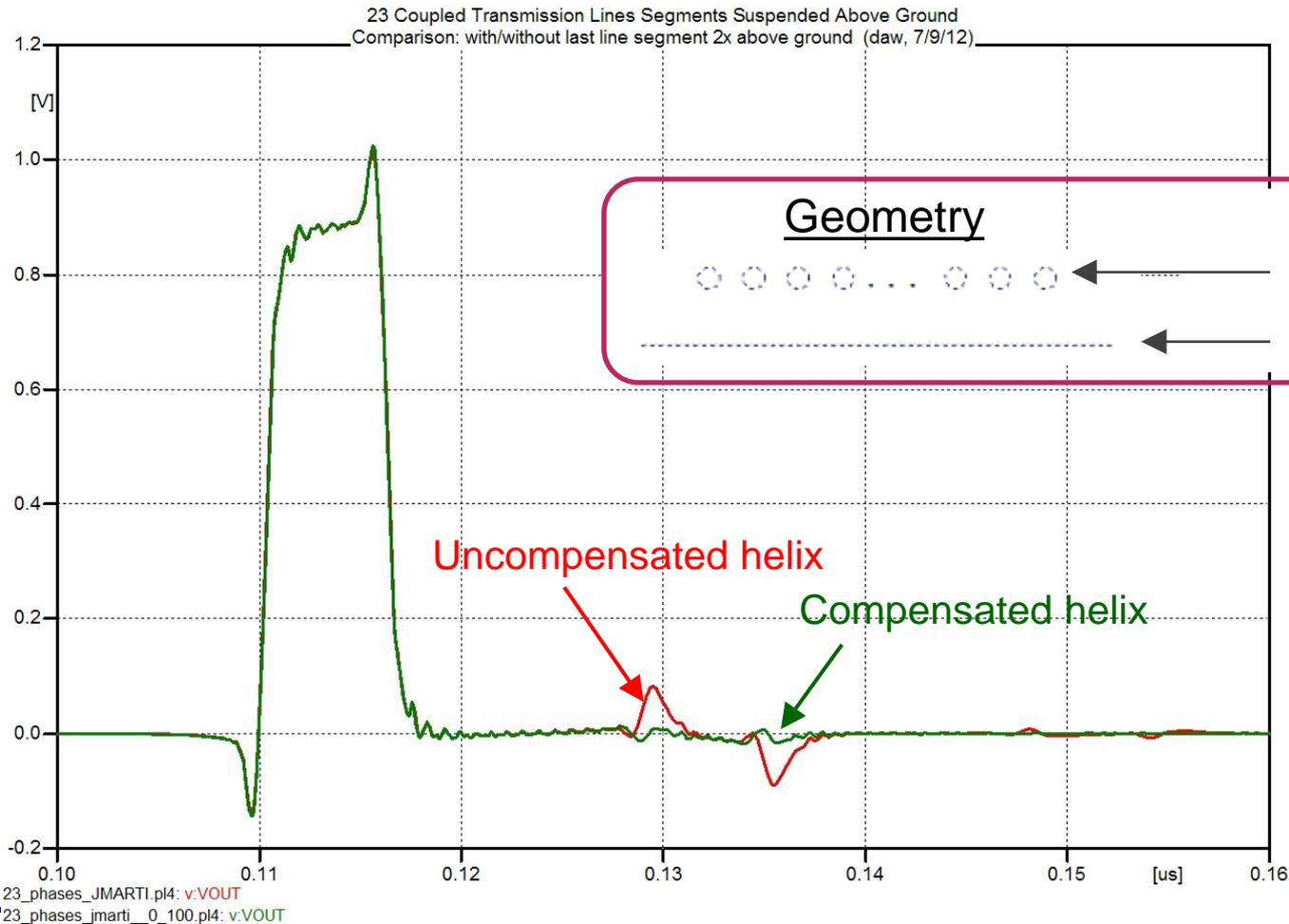


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- Low capacitance (200 Ω) feed throughs are on order
 - Work on the driver up until April has suggested the feasibility of designing a multiple FET cascode switch
 - Bench testing has been done up to 500V
 - 480 V pulses were demonstrated
 - Work remains
 - Driver's power dissipation seems manageable
 - GaN FETs are very attractive switching transistors
 - Sub-nanosecond rise/fall times are achievable
 - Voltage testing of 200 V rated parts from Polyfet Devices
 - One GP141 ran >several weeks switching 100V, 1.25 A at 27 MHz
 - One GP141 broke switching at 150 V
 - Alex Chen has progressed as far as possible awaiting modeling results from Technical Division
 - There is no update from SLAC (maybe on vacation?)
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- Regarding TDR impedance measurement of the 200 Ω prototype
 - Known: helix impedance is ~50% higher than flat microstrip line with same wire-to-ground spacing
 - Observation: impedance tapered from the ends toward the center ~50 Ω
 - Howie Pfeffer's Speculation: last turn has less inter-winding coupling
- Model the helix to look for a correlating trend (Howie & Dan Wolff)
 - Construct 23 flat line segment model using EMTP
 - Each helical turn is straightened out to be flat in this model
 - Wire-wire and ground geometry are made similar to prototype
 - Line segments are interconnected with 0 Ω , zero length shorts
 - EMTP computes inter-winding coupling
 - Each line segment includes .5 pF electrode capacitance to ground
- Compensated model
 - Last (23rd) "turn" wire-to-ground space doubled

Helix model – Compensating the last turn



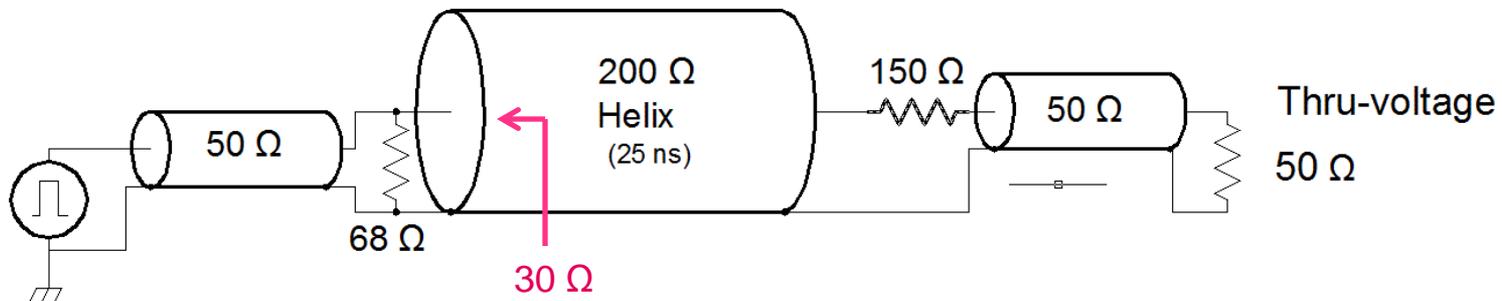


- Objective: measure reflections from components downstream of the helix
 - 200 Ω load
 - Fabricated 200 Ω transition line
- Motivation
 - Mismatches downstream of the helix cause reflections
 - Low impedance bipolar switch causes re-reflections
 - Re-reflected voltage travel through the kicker with the beam
- Measurement technique of component mismatch
 - Drive helix with a 50 Ω generator (reasonably low impedance)
 - Reflection coefficient is .75 versus .95 for bipolar switch
 - Observe the incident through-voltage out of the helix
 - Install downstream components
 - Observe through-voltage out of the load
 - Any voltage differences 50 ns after the generated signal are re-reflections of component impedance mismatch

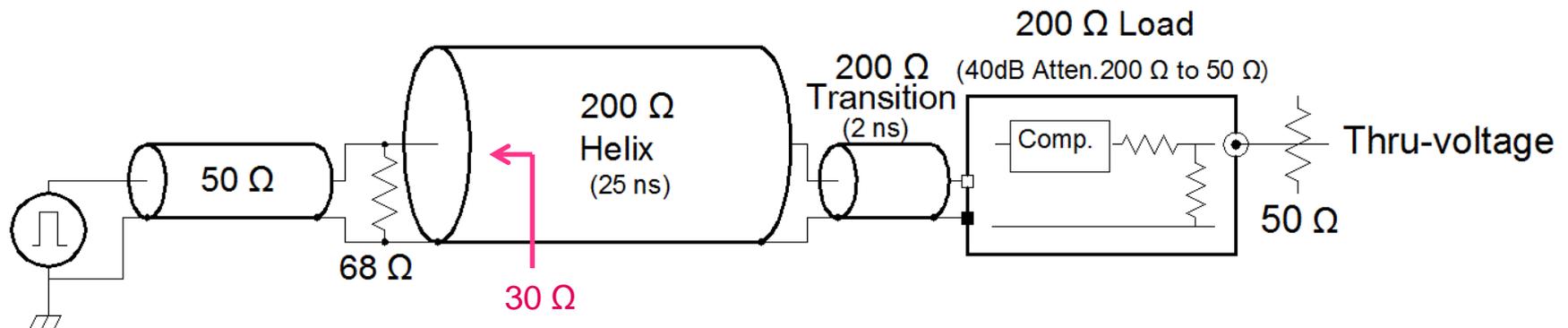
Reflection test setup



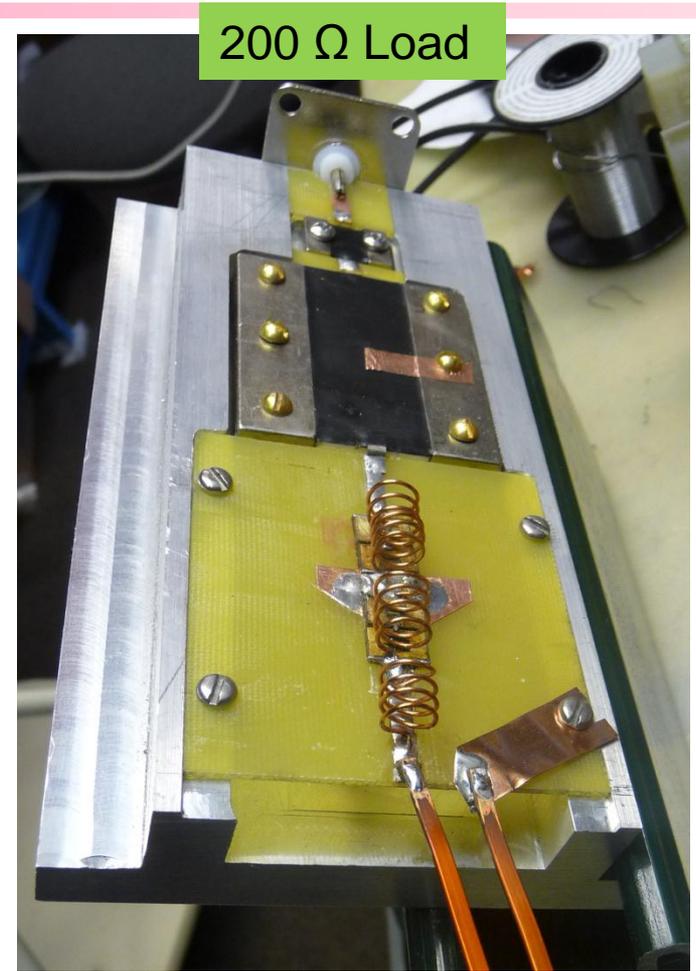
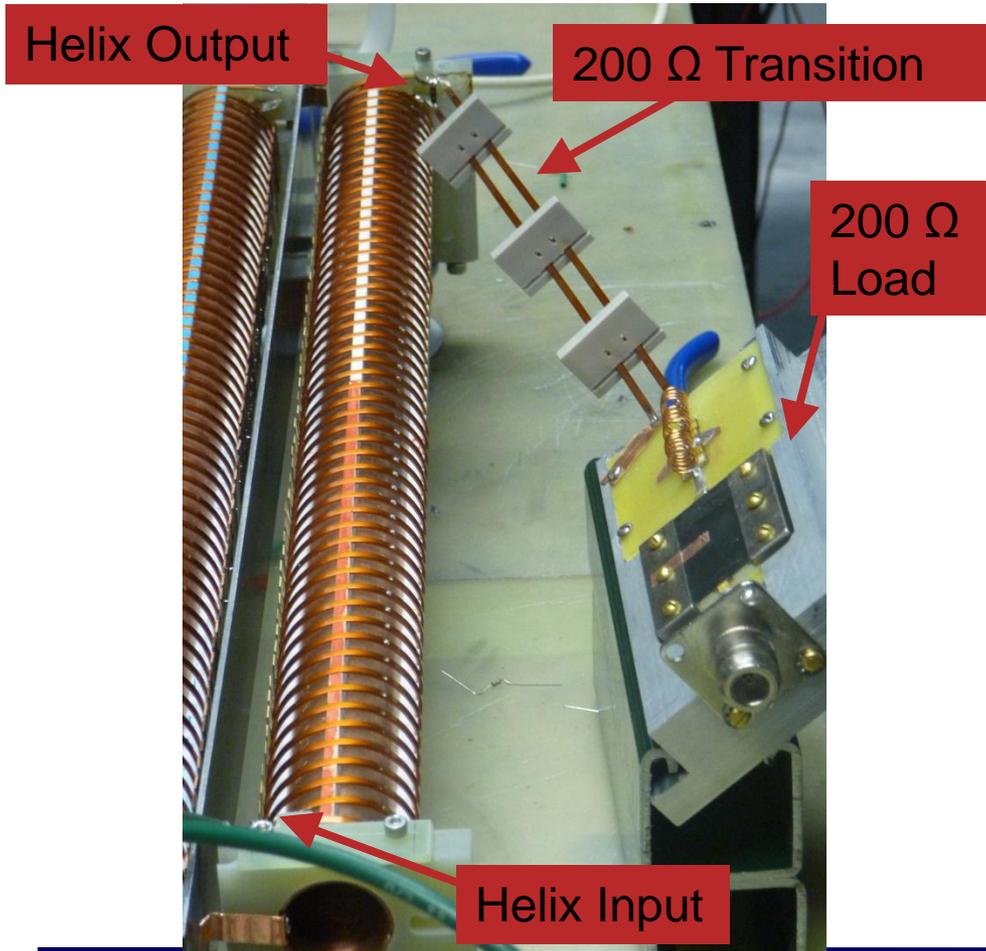
Helix Only (reflection free reference signal)



Helix + 200Ω transition + load



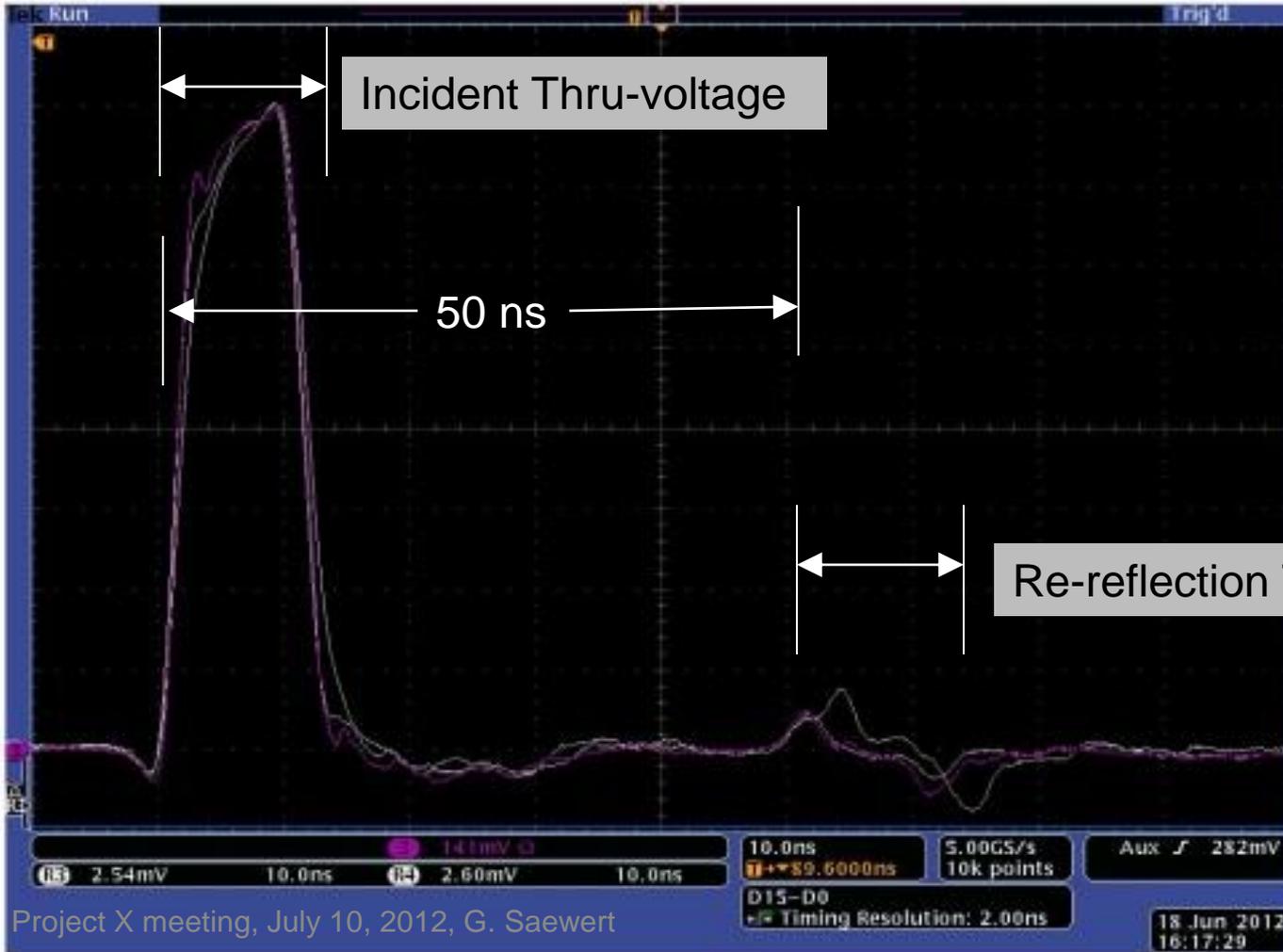
Connected load



Through-voltages

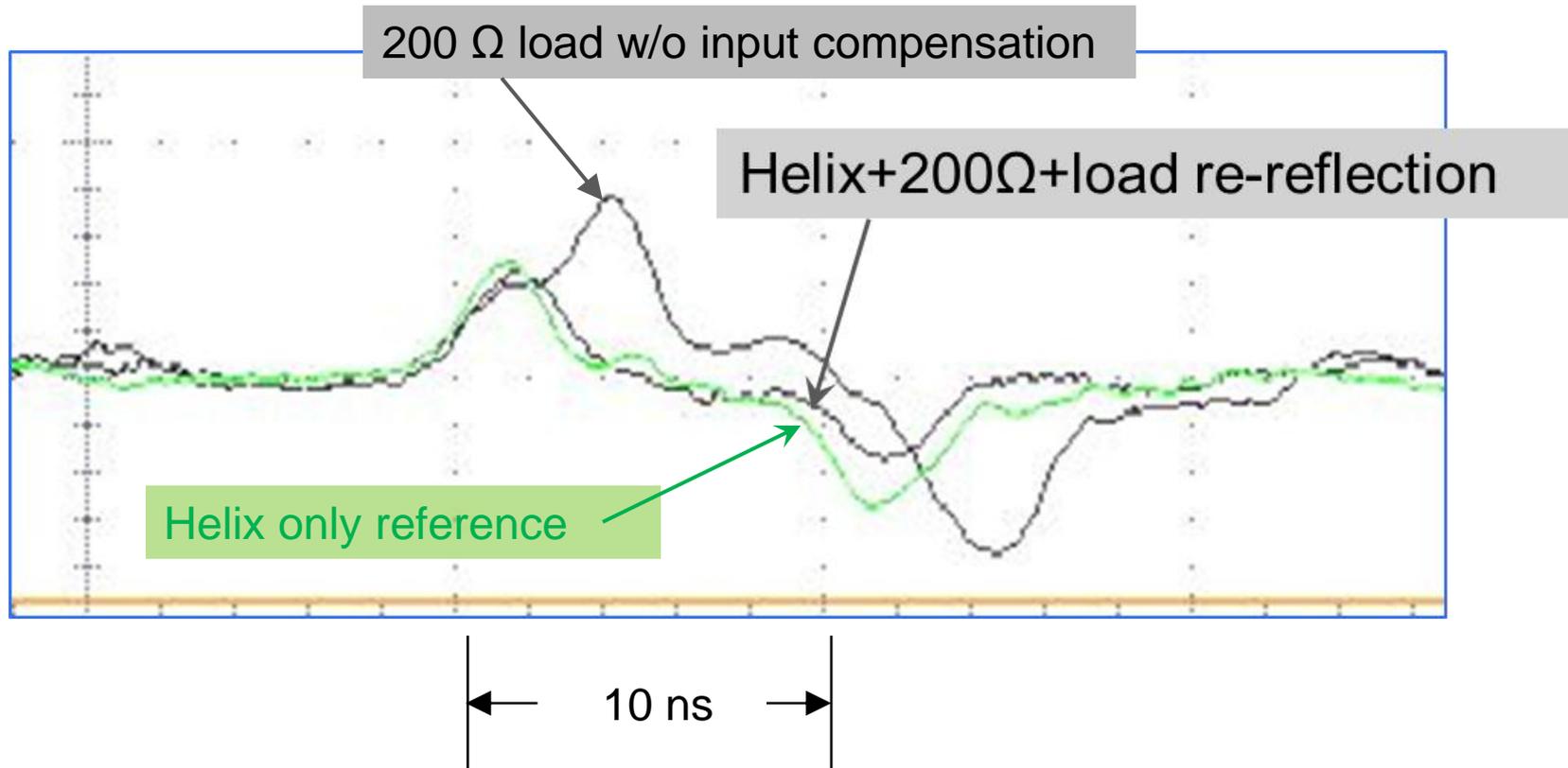


Home: MSO4104B 0800111efbfab (131.225.136.4)



10 ns wide pulse

Re-reflections (zoomed in)

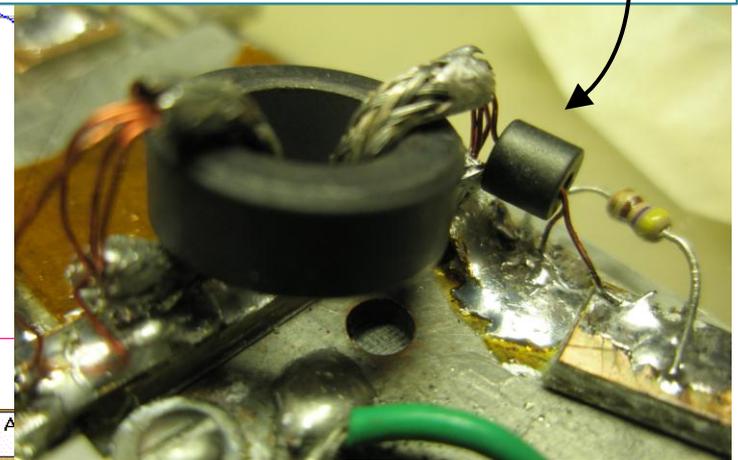
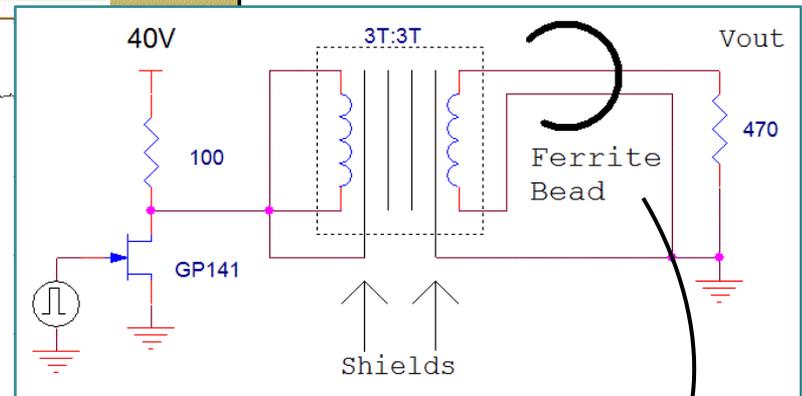
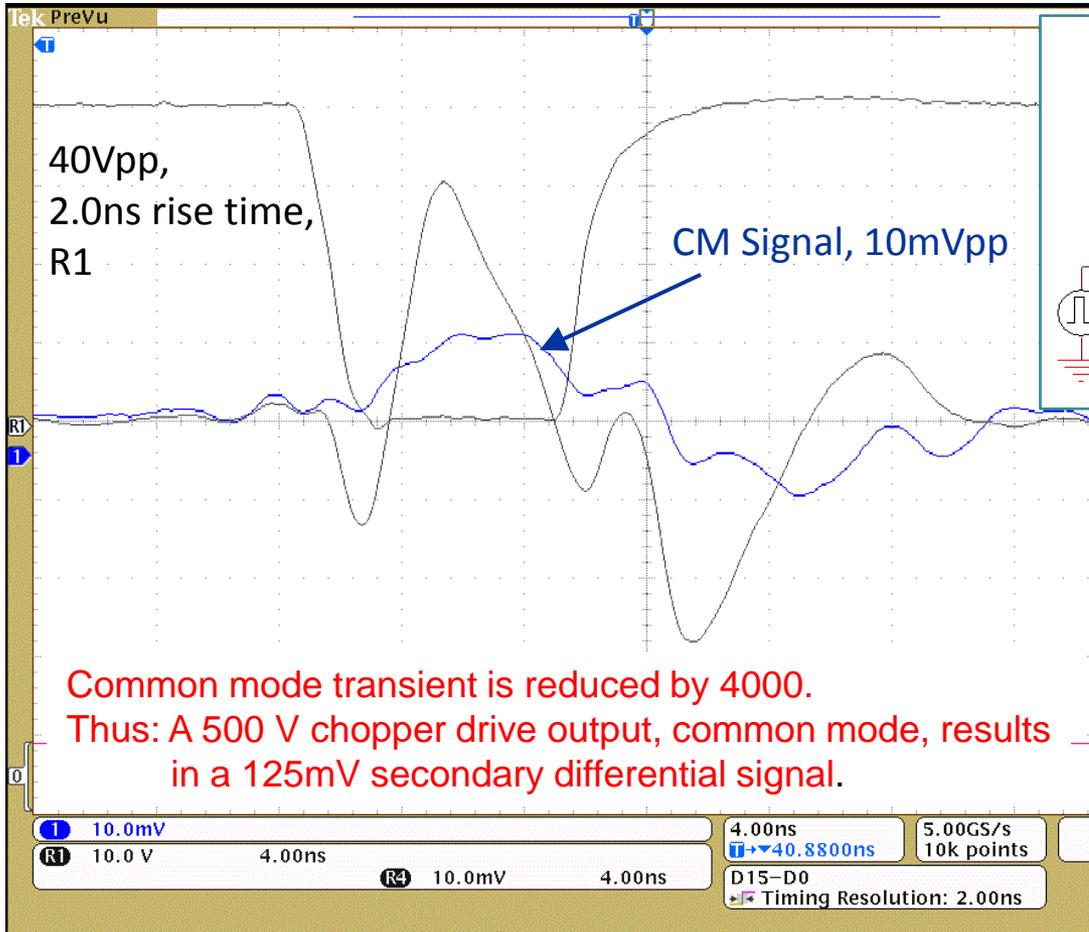


Bipolar switch – drive isolation considerations



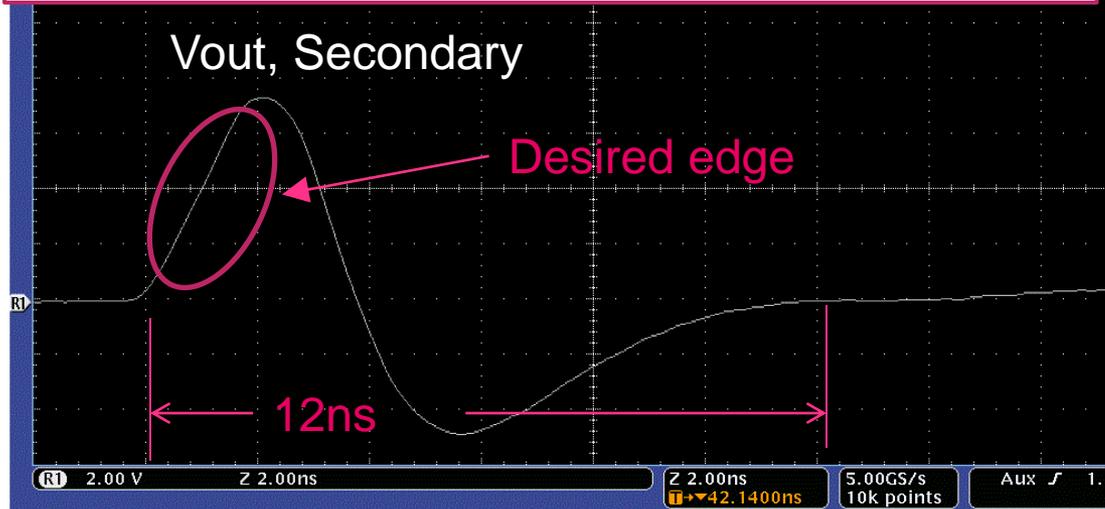
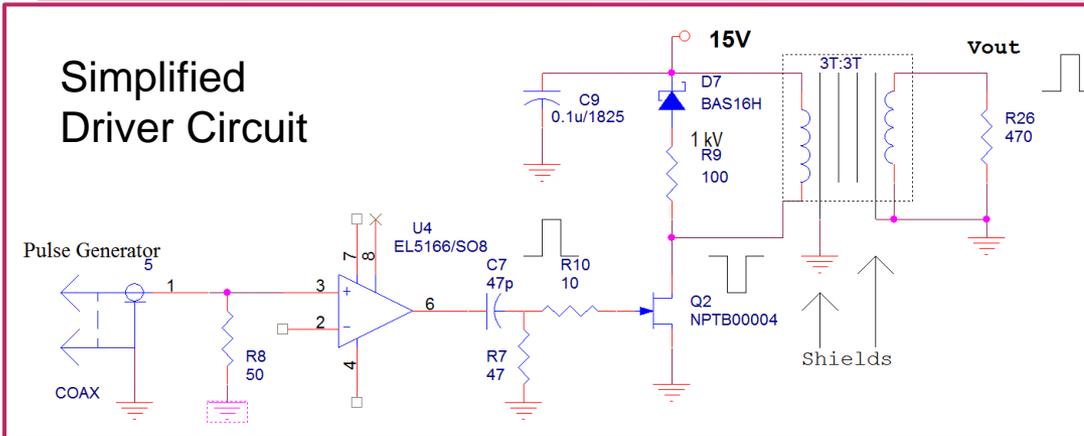
- Bipolar switch drive isolation issues
 - Jitter
 - Low to high side capacitive coupling causing common mode transients
250 – 500 kV/ μ s (x10 silicon isolator capability)
 - Wide switch gate pulse width range
3 – 1000 ns
- design options
 - High speed fiber optic transceivers
 - Pros: (1) fast (.1 - .4 ns rise/fall times)
(2) infinite common mode transient immunity
 - Cons: (1) jitter (>1 ns)
(2) large parasitic capacitance to ground
(e.g. 1 pF @ 500V/ns adds .5 A of switch current)
 - Transformer coupling
 - Pros: no jitter
 - Cons: (1) high transient immunity and voltage rating is not available in a commercially available transformer
(2) parasitics (?) - capacitance to ground and common mode
(3) speed (?) – rise/fall time and time to rest the core

Isolation transformer design - common mode transient immunity



Doubly-shielded pulse transformer

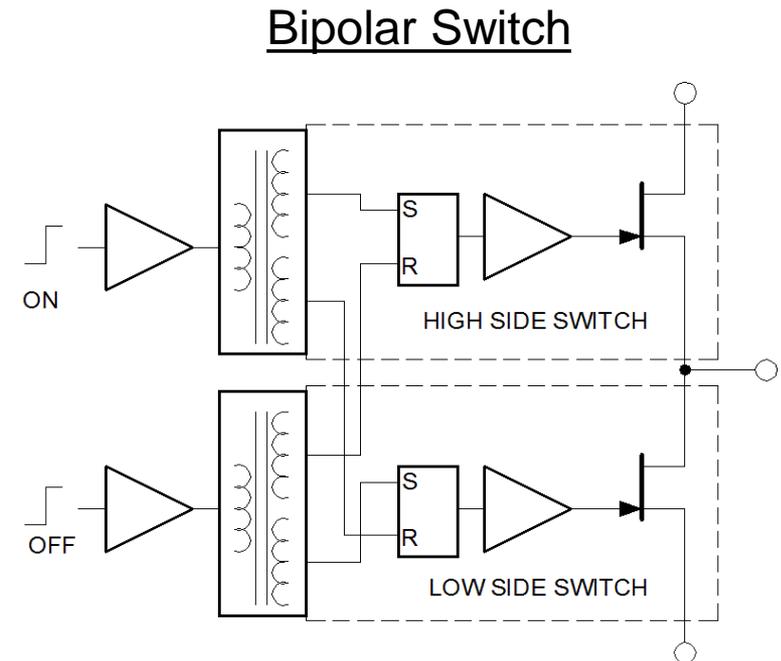
Isolation transformer design - remaining issues



- Designing for high CM transient immunity is #1 priority
 - Enhance it by generate a large voltage and divide it down on the secondary
- Minimize CM capacitance
 - Transformer physically small
 - Separate the two shields
 - This design: 0.22 pF CM
- Designing for high CM transient immunity and speed precludes wide gate widths
 - Separated primary and secondary increases leakage inductance
 - Leakage inductance slows down the pulse
 - Design to communicate only an “edge”
- Design for speed
 - Reduce number of turns
 - Minimize leakage inductance
 - Secondary rise time is $L_{leakage}/R_{sec}$
 - Minimize primary side capacitance
 - Core reset recovery time is L/C resonant
- Final result: triggerable at 80MHz



- Design includes two isolation transformers having two secondaries
 - Both secondaries are isolated from each other on each core
 - Provides reliable timing to assure one switch turns off when the other turns on
 - The edges of ON and OFF signals close either of the two switches



Proposed chopper system testing



- Measure electric field by use of probes
- Options
 - Probe between two helixes
 - Measure voltage on insulated “electrodes” insulated from ground plate located at beam center
 - Compute electric field from voltage and measured electrode capacitance
- Measuring and different locations along the kicker and calculate an integral
- Delay can be measured with oscilloscope probes



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- Paired-strip, flat wire 200 Ω transmission lines do not present reflection problems
 - 200 Ω load prototype meets VSWR spec
 - As is, it requires to be outside the vacuum
 - Its compensation network probably requires air cooling
 - Isolation transformer design issues have been resolved
 - Common mode transient immunity
 - speed